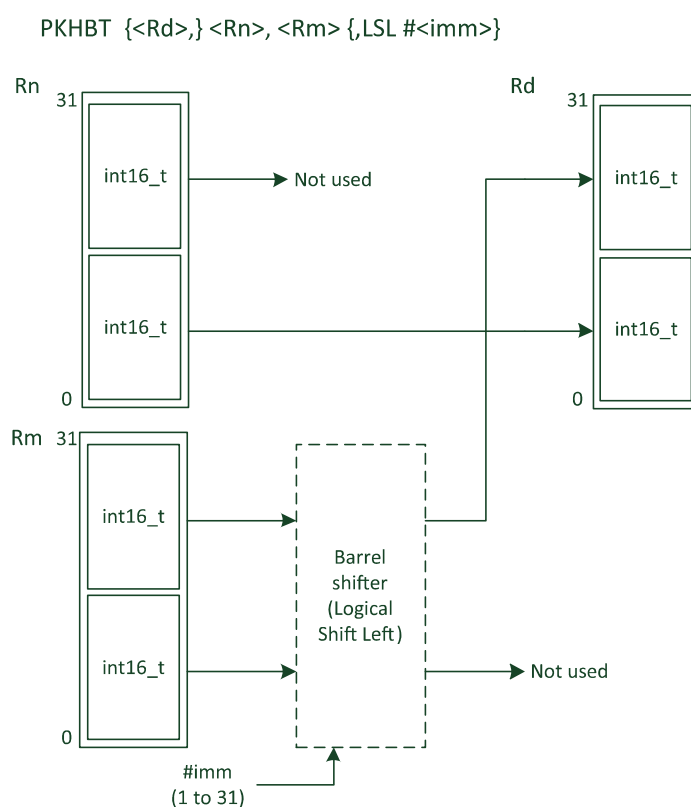


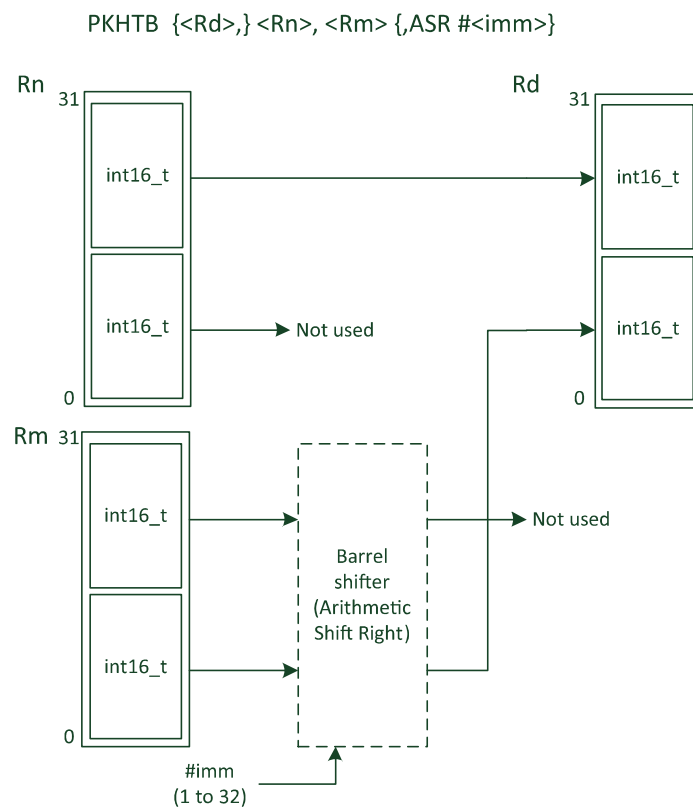
# Graphical Representations of DSP Instructions

This appendix contains graphical representations of the Enhanced DSP instructions in ARM Cortex<sup>®</sup>-M4 Processor. See section 5.7 for details, and appendix section A.2 for summaries.



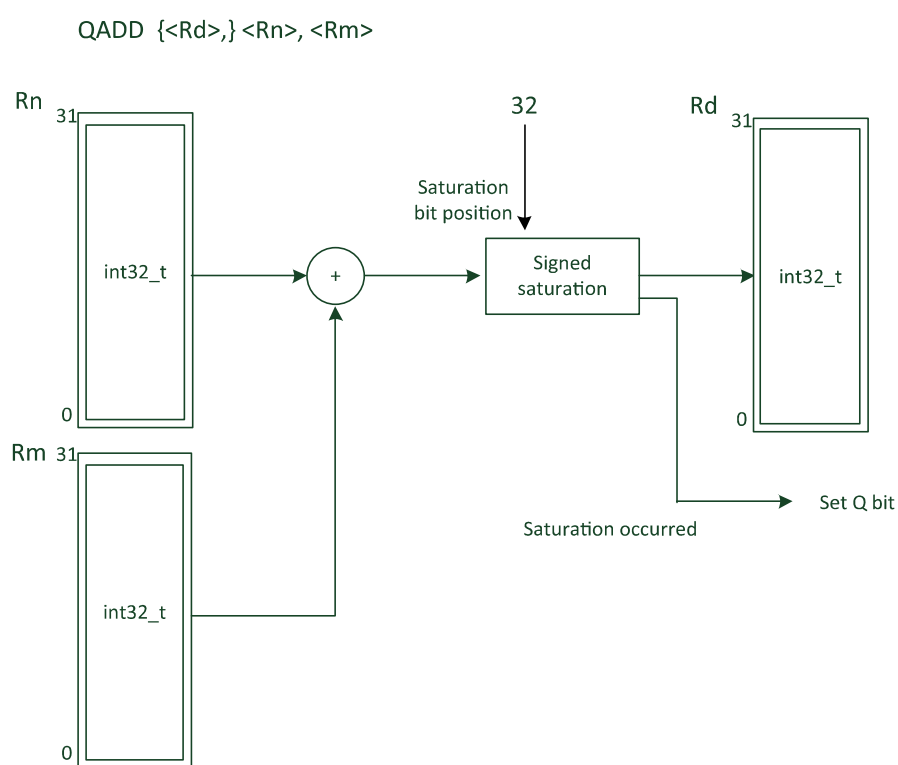
**FIGURE B.1**

PKHBT

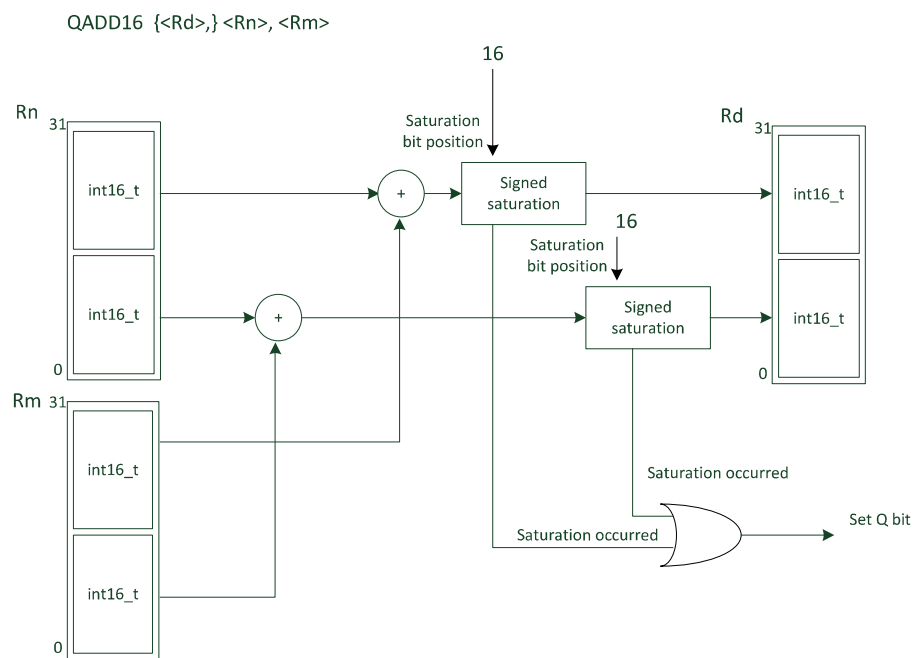


**FIGURE B.2**

PKHTB



**FIGURE B.3**  
QADD



**FIGURE B.4**

QADD16

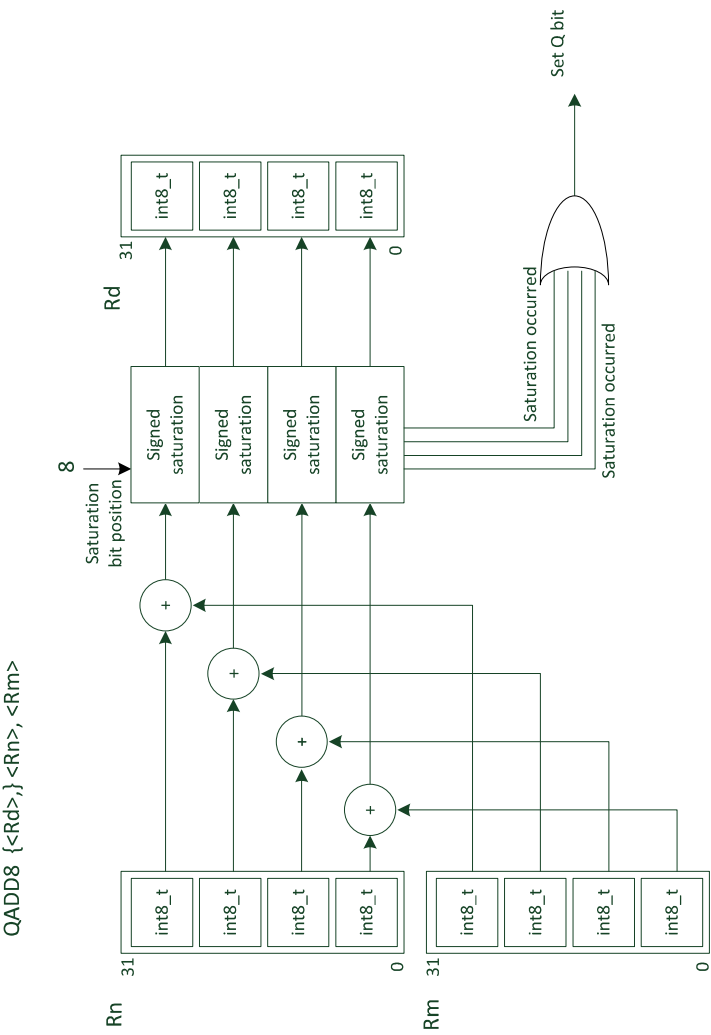
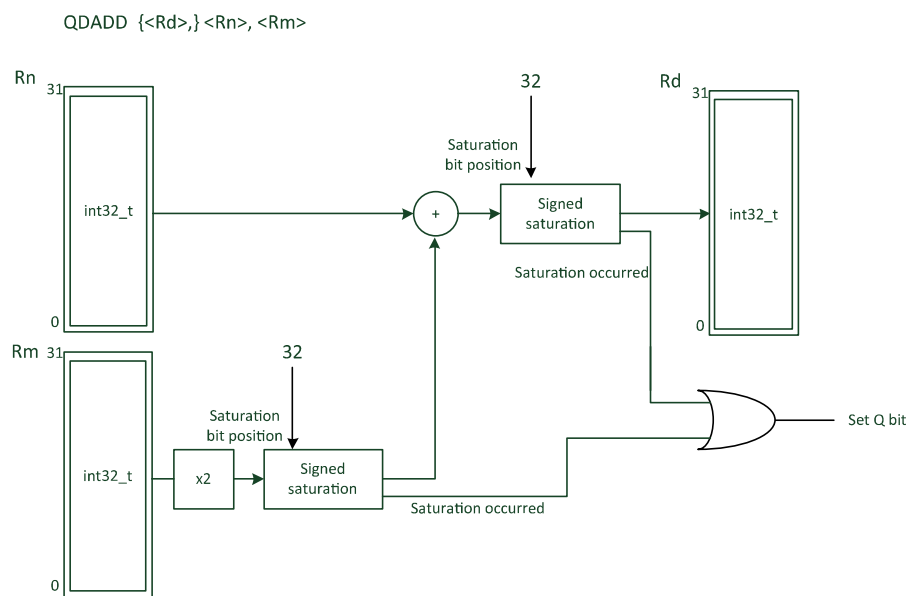
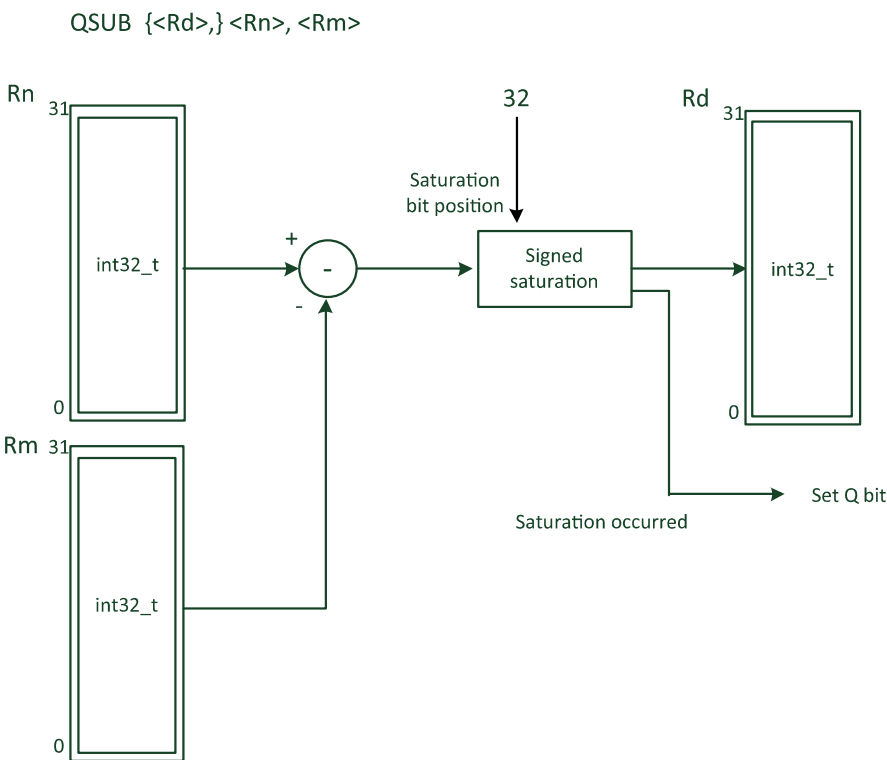


FIGURE B.5  
QADD8

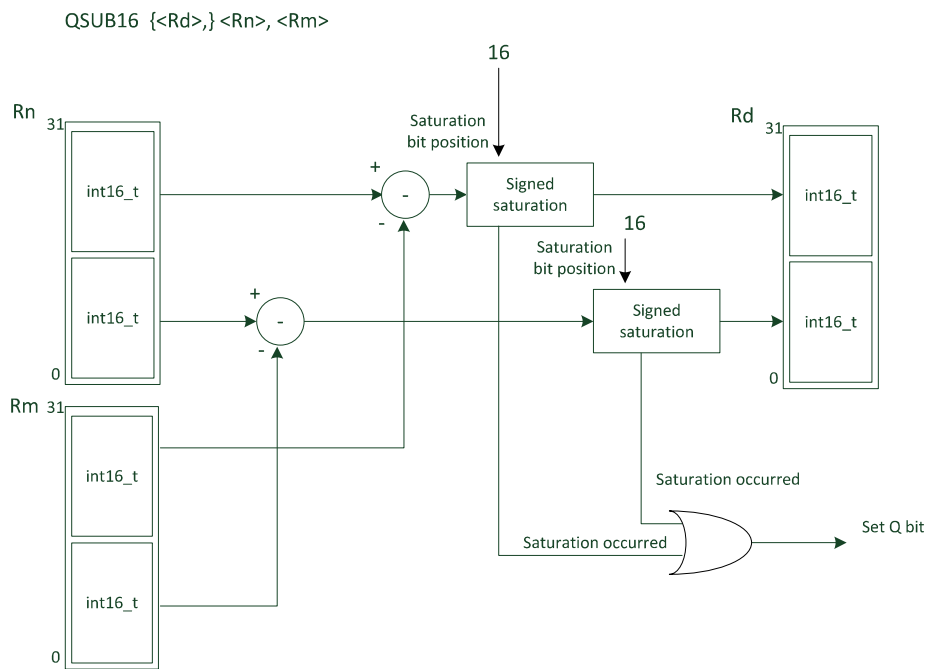


**FIGURE B.6**

QDADD



**FIGURE B.7**  
QSUB



**FIGURE B.8**  
QSUB16



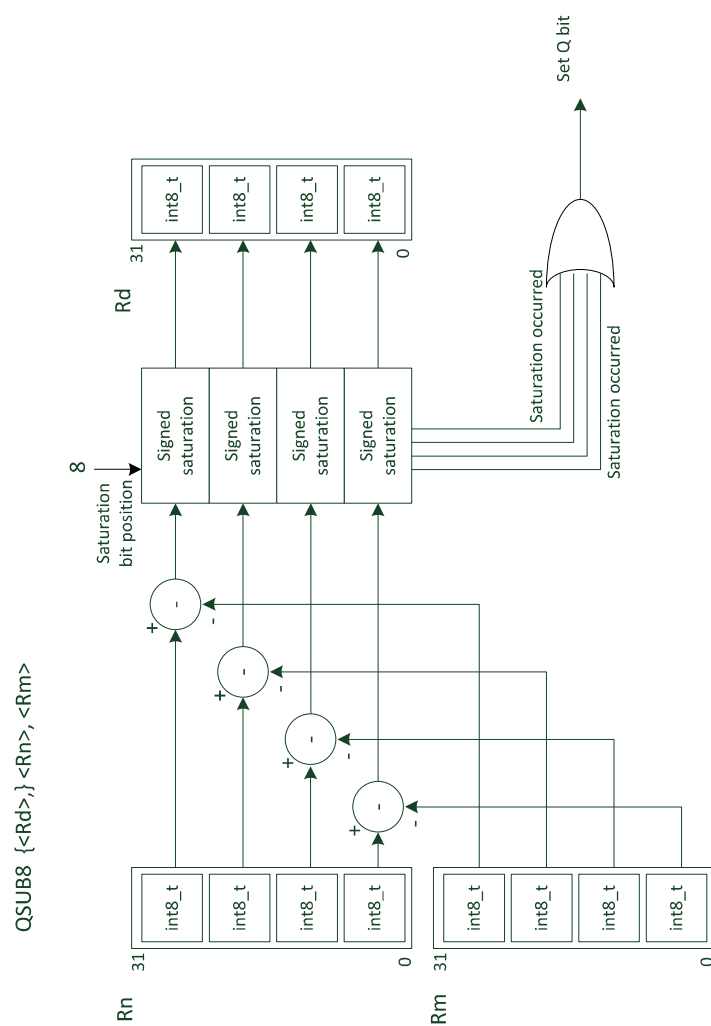
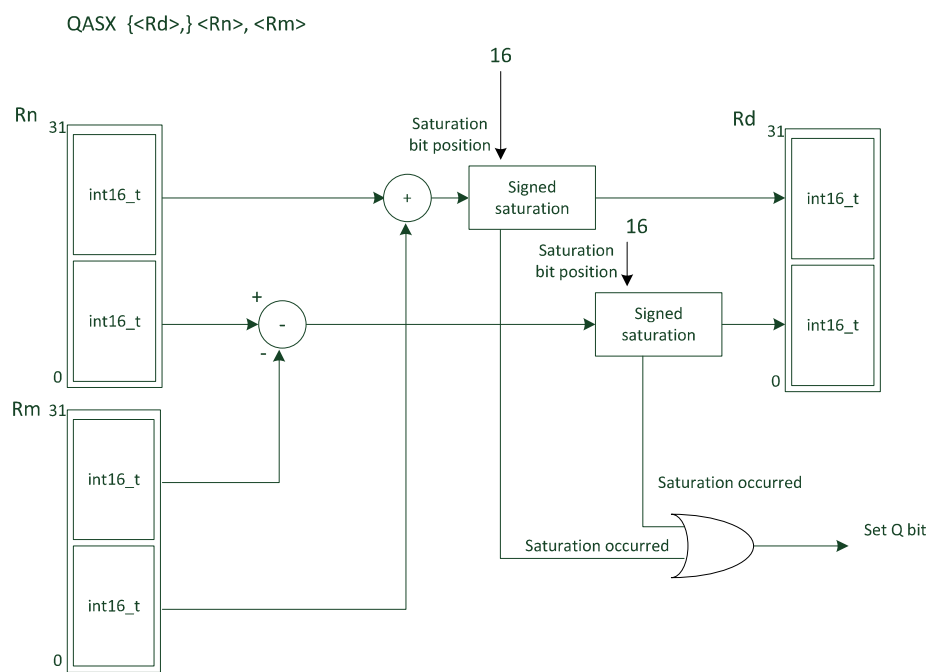
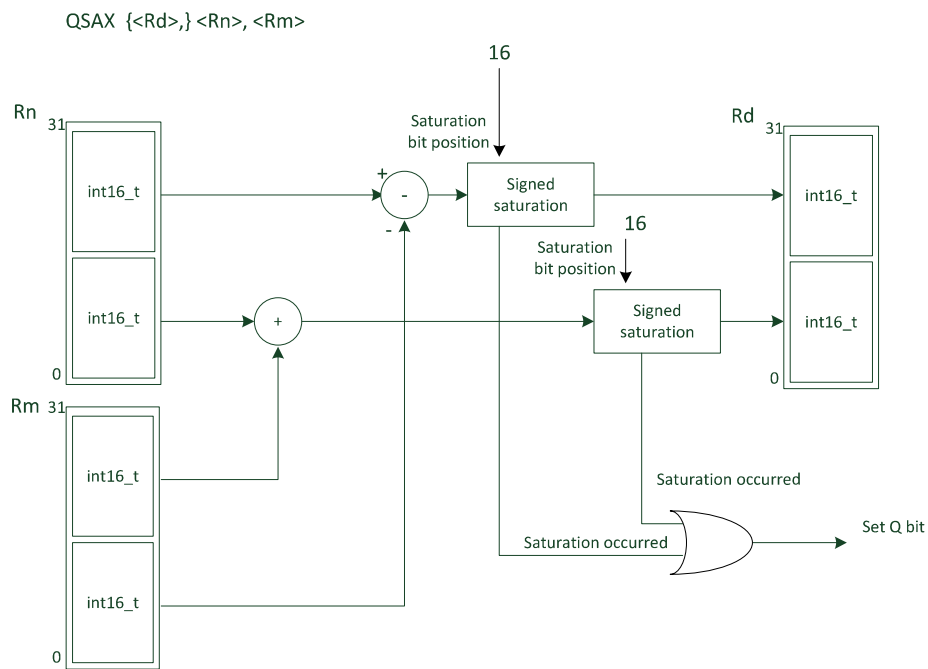


FIGURE B.9  
QSUB8



**FIGURE B.10**  
QASX



**FIGURE B.11**  
QSAX

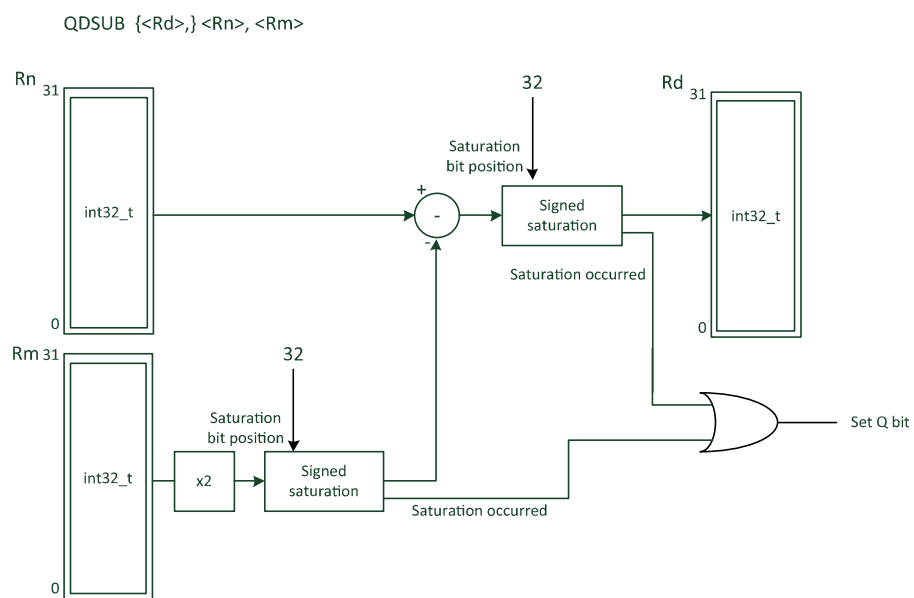


FIGURE B.12

QDSUB

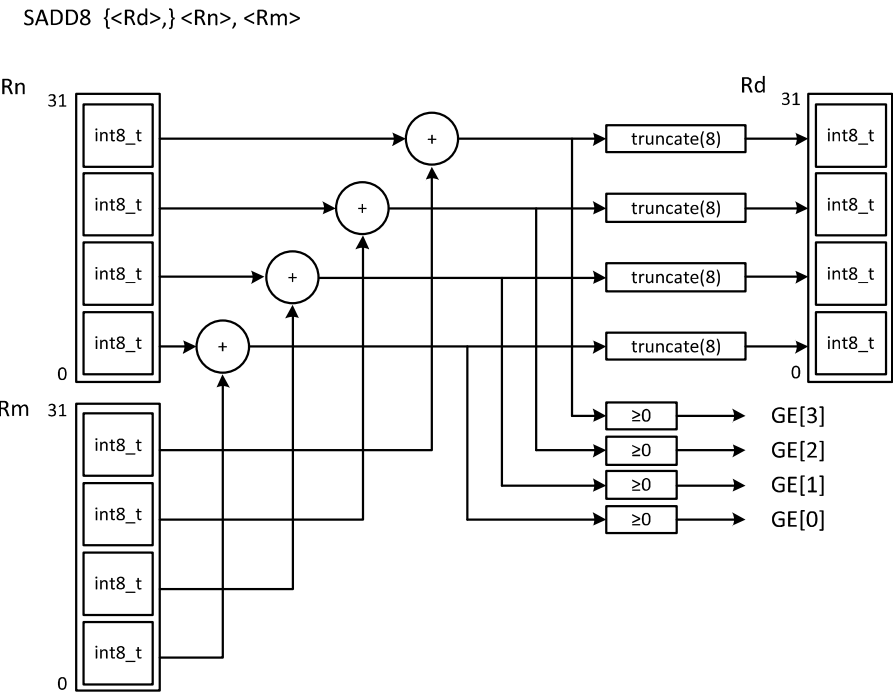
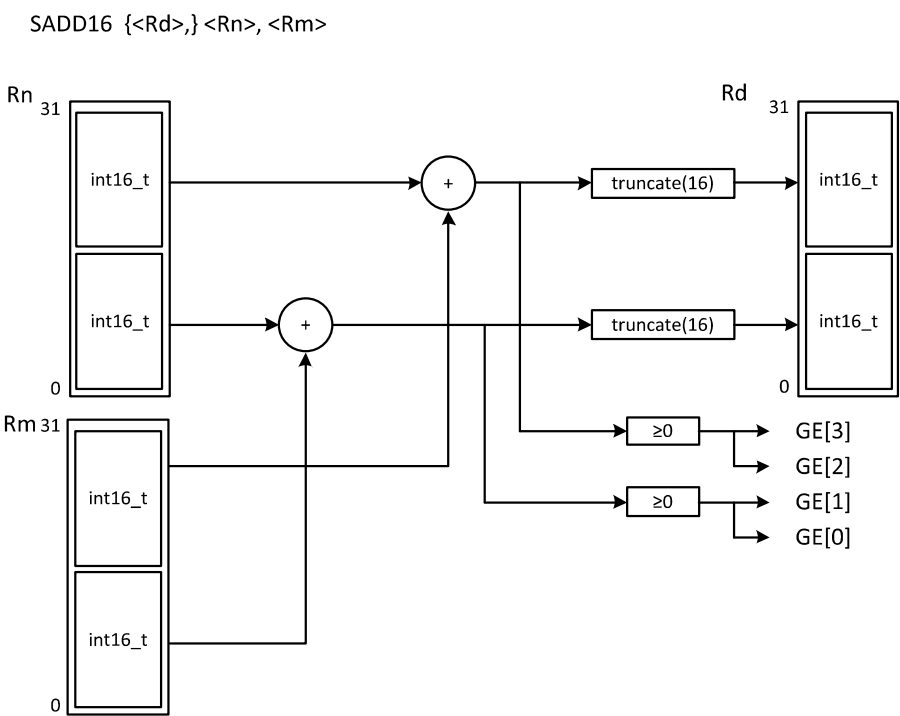
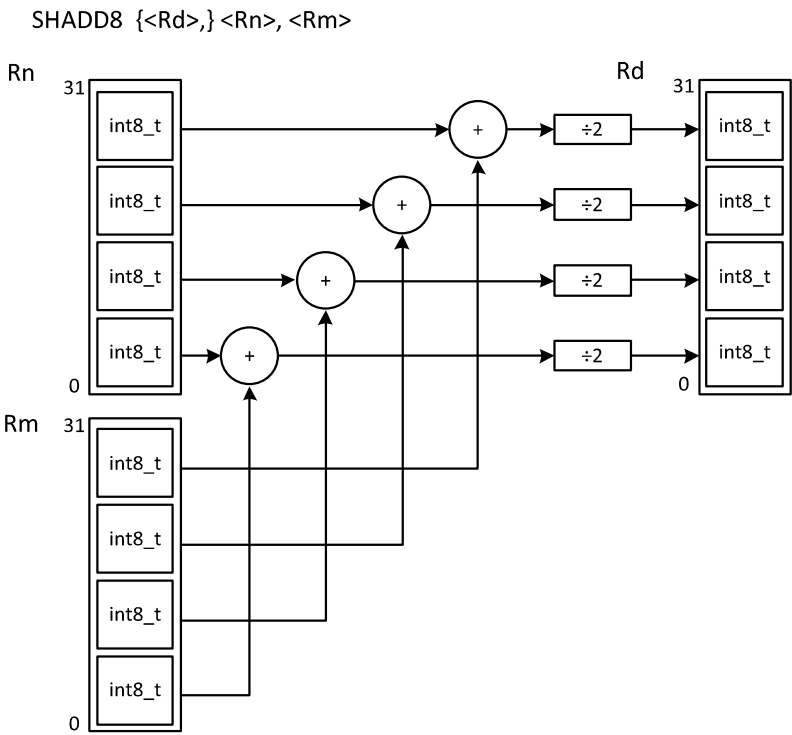


FIGURE B.13

SADD8



**FIGURE B.14**  
SADD16



**FIGURE B.15**  
SHADD8

SHADD16 {<Rd>,}<Rn>, <Rm>

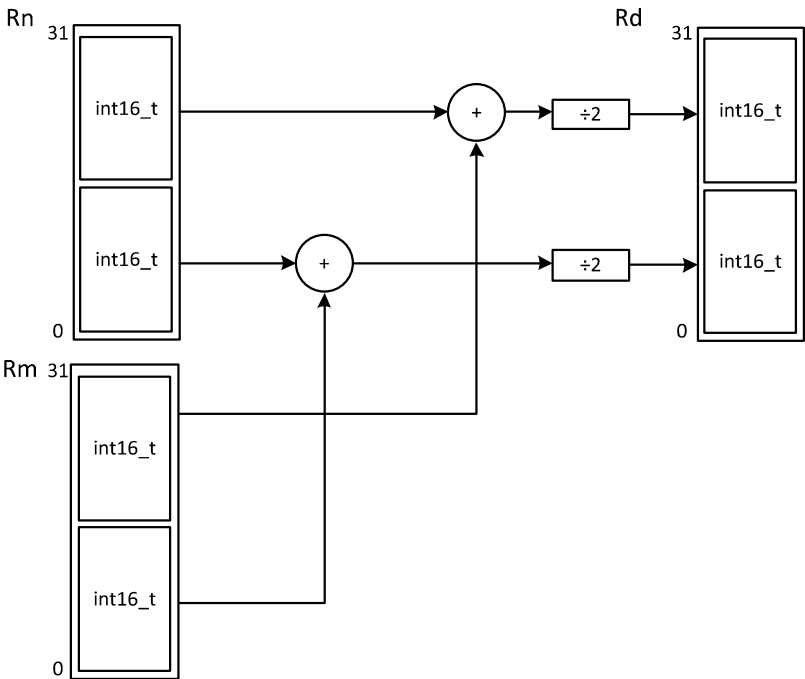


FIGURE B.16  
SHADD16



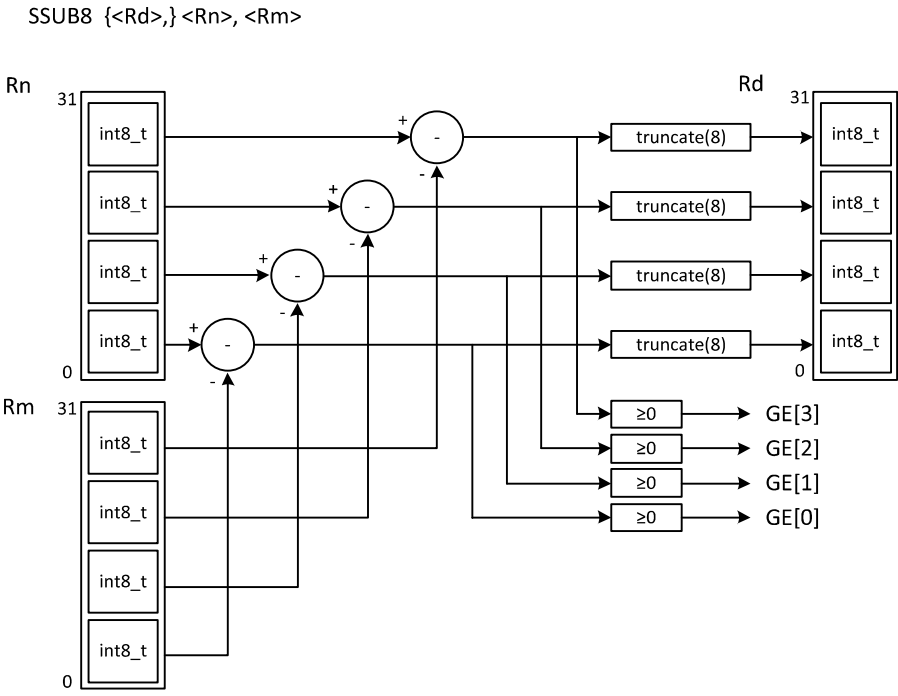
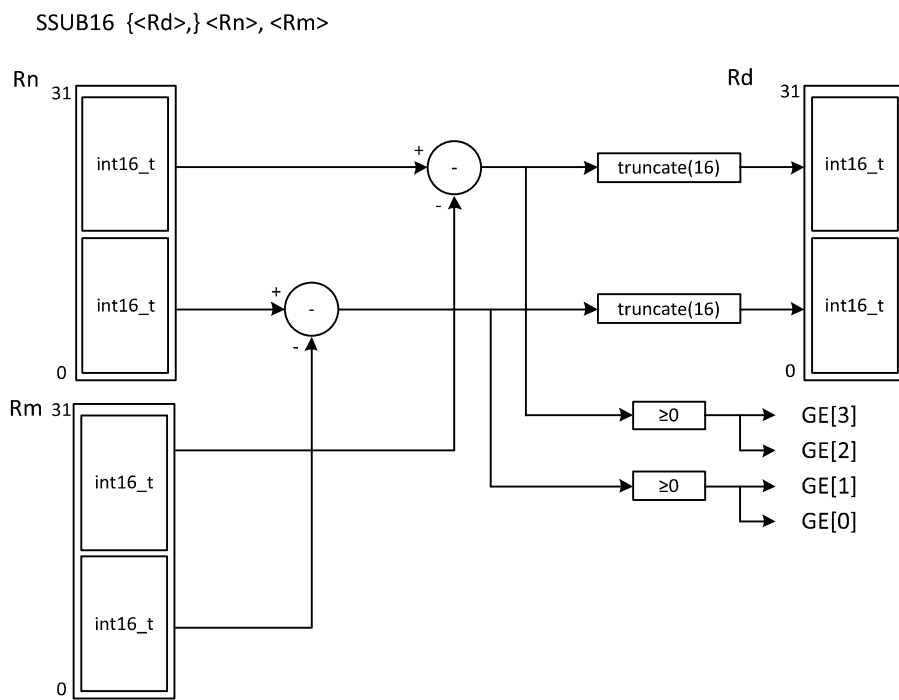


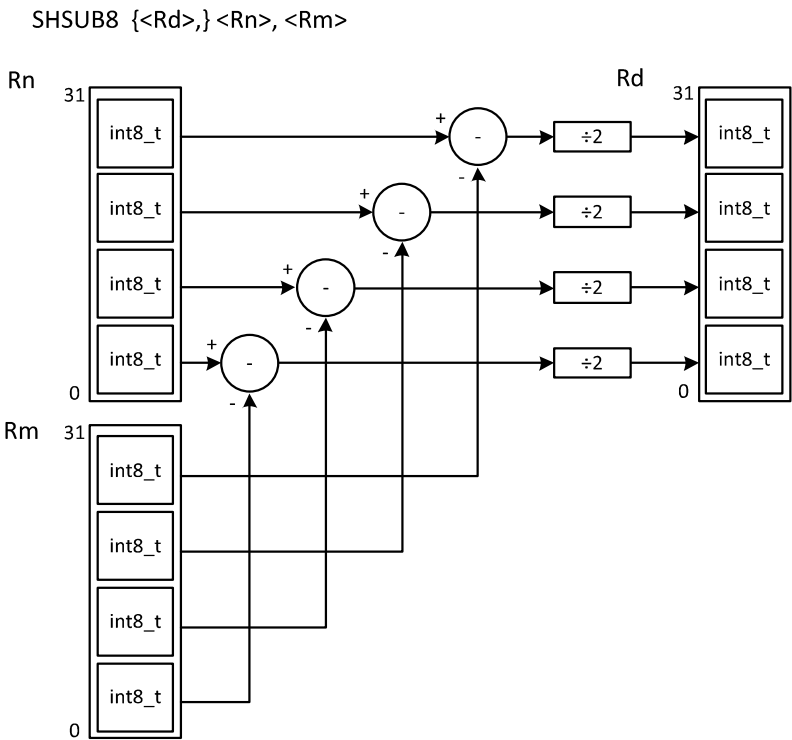
FIGURE B.17

SSUB8

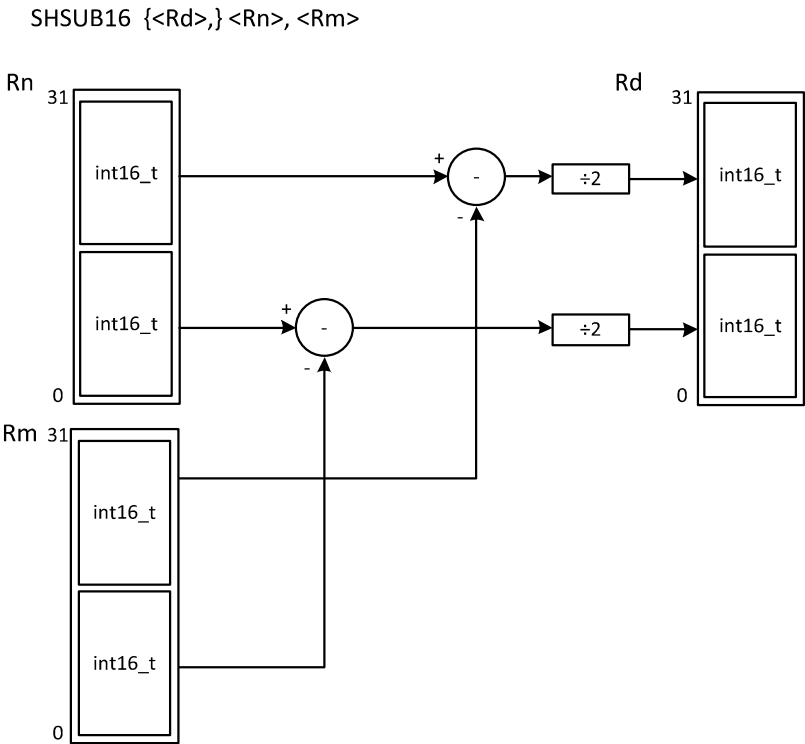


**FIGURE B.18**

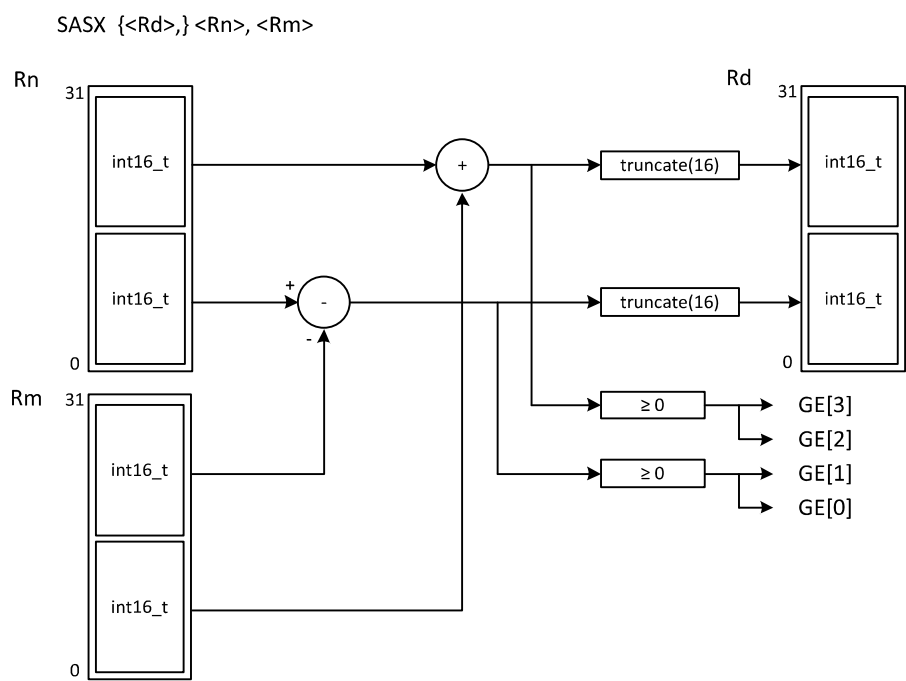
SSUB16



**FIGURE B.19**  
SHSUB8

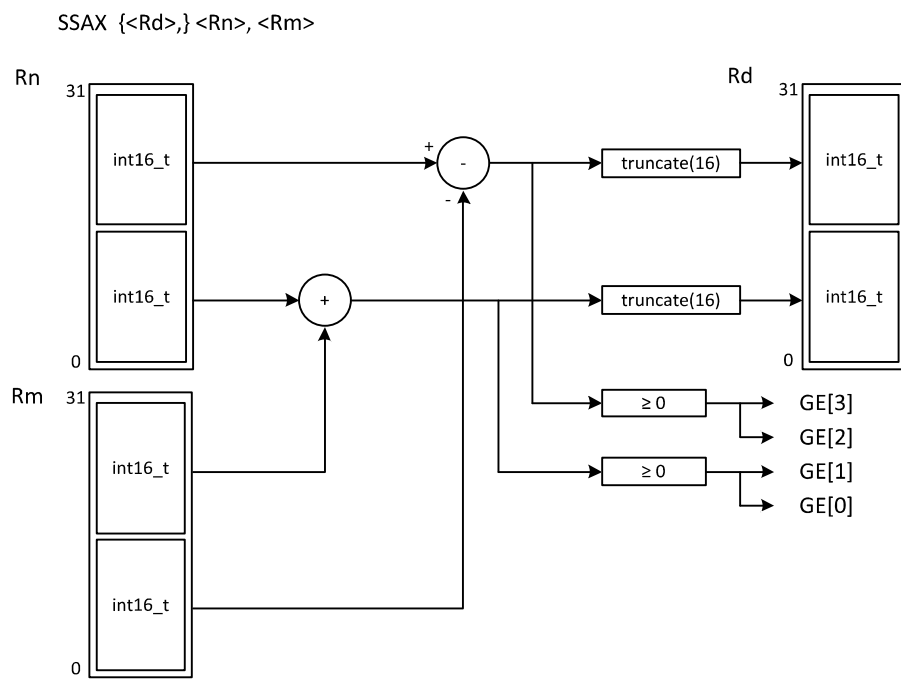


**FIGURE B.20**  
SHSUB16



**FIGURE B.21**

SASX



**FIGURE B.22**

SSAX

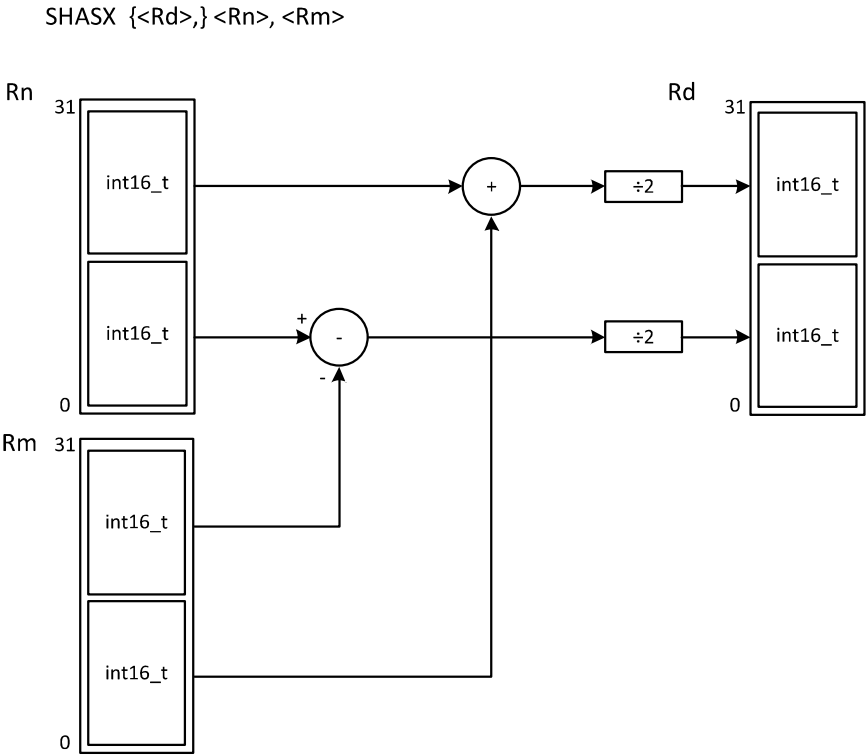


FIGURE B.23

SHASX

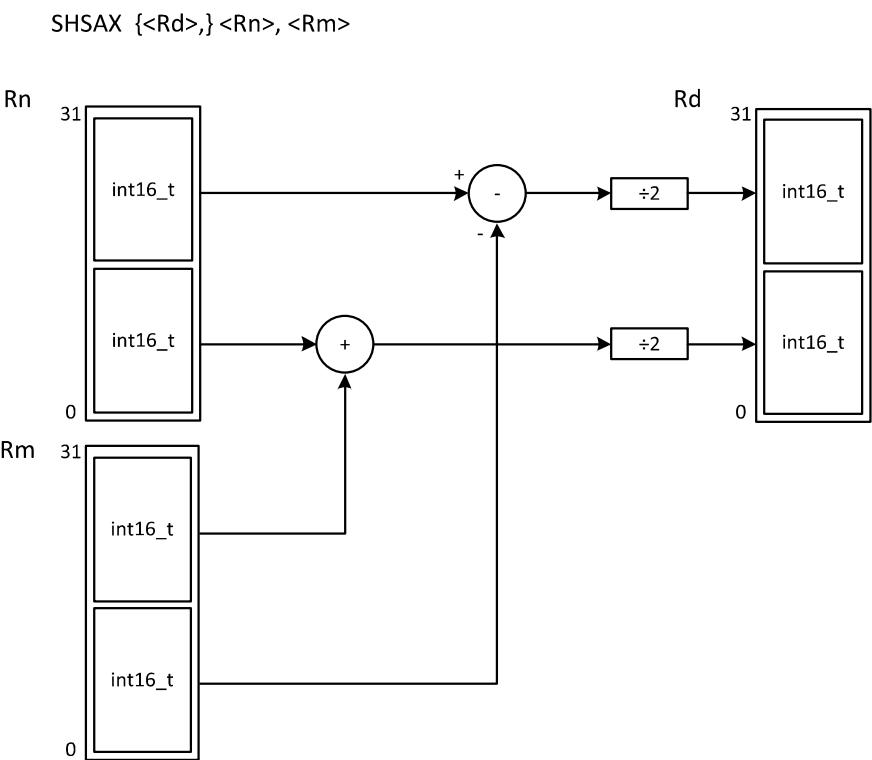
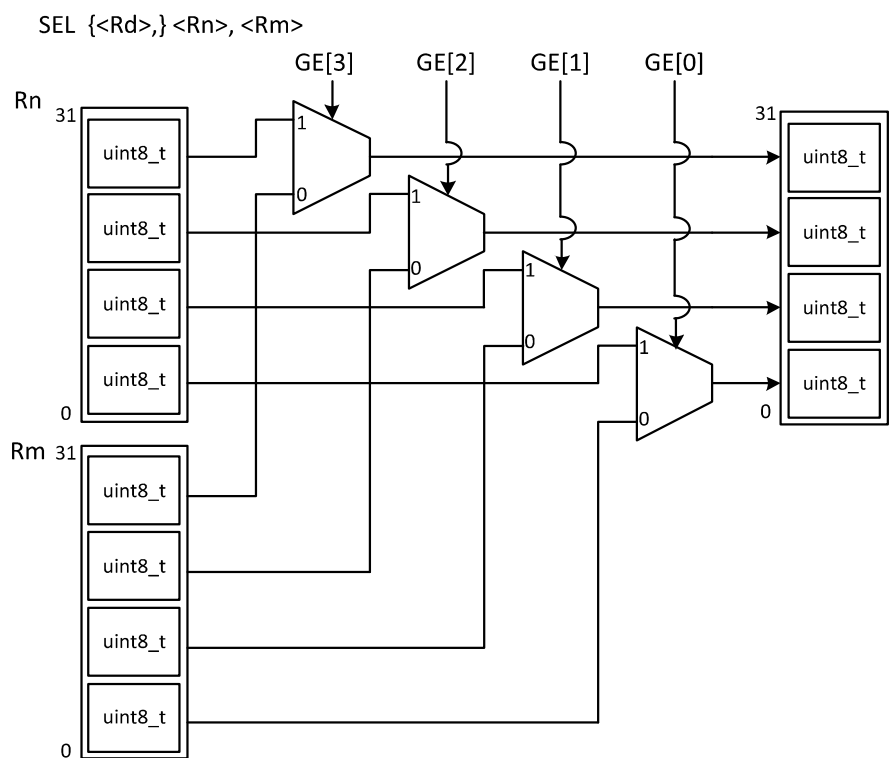


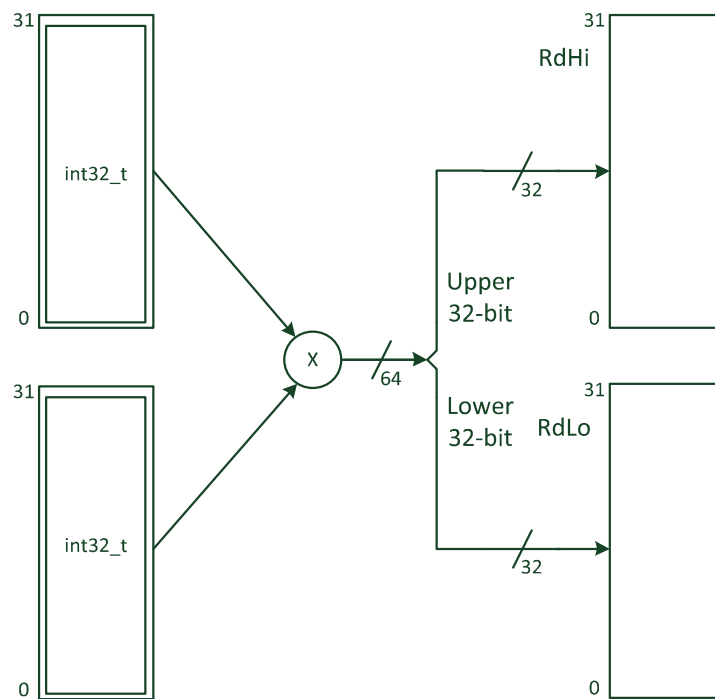
FIGURE B.24  
SHSAX





**FIGURE B.25**  
SEL

SMULL <RdLo>, <RdHi>, <Rn>, <Rm>  
(available in the Cortex-M3)



**FIGURE B.26**  
SMULL

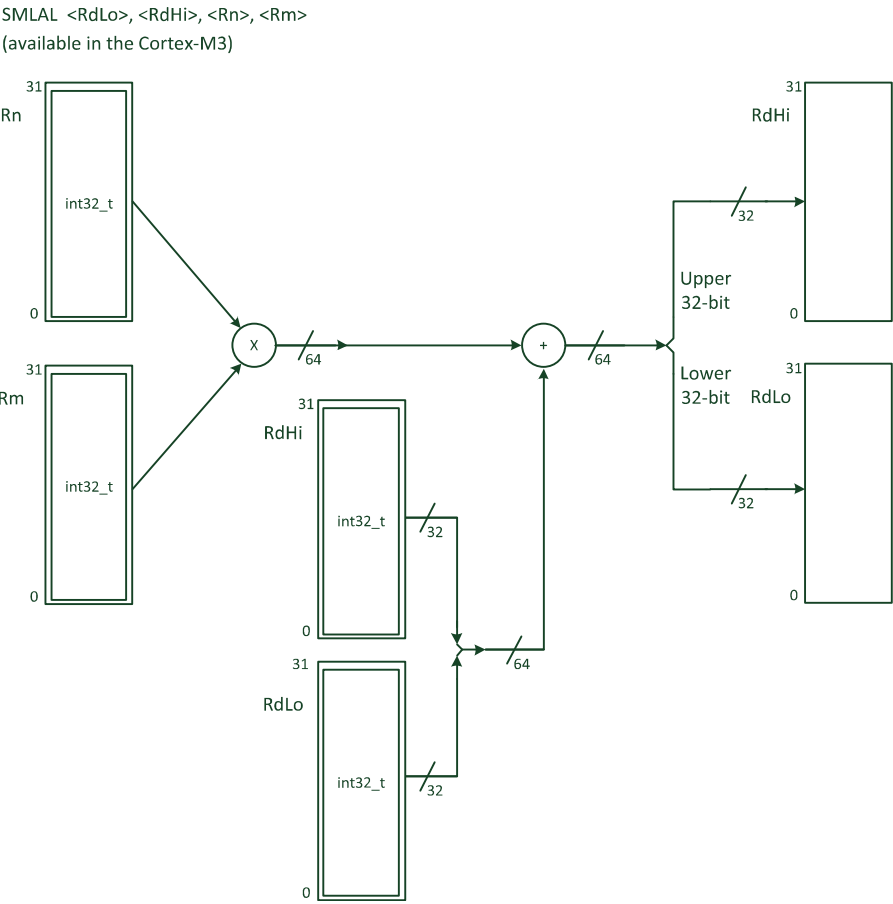
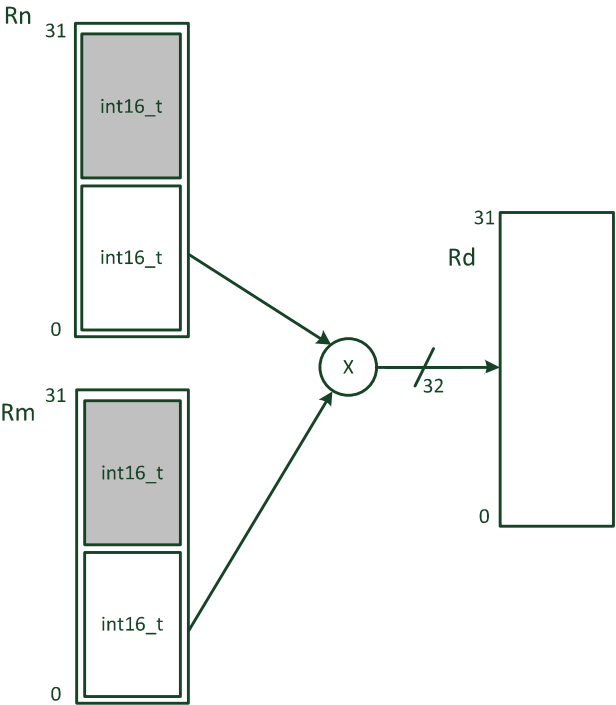


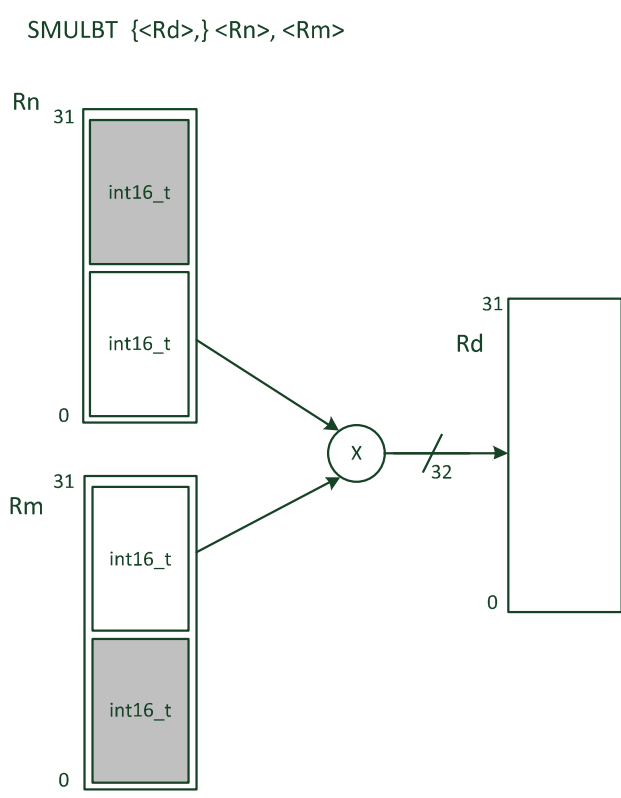
FIGURE B.27

SMLAL

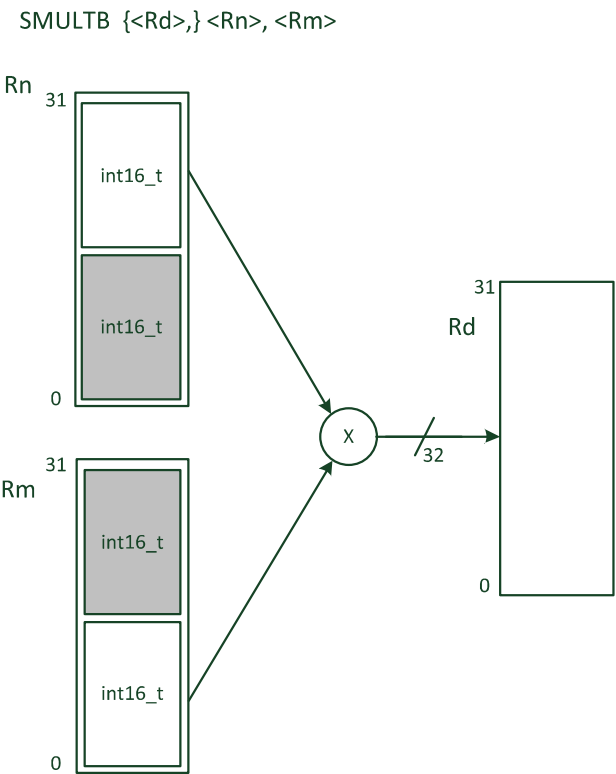
SMULBB {<Rd>,} <Rn>, <Rm>



**FIGURE B.28**  
SMULBB

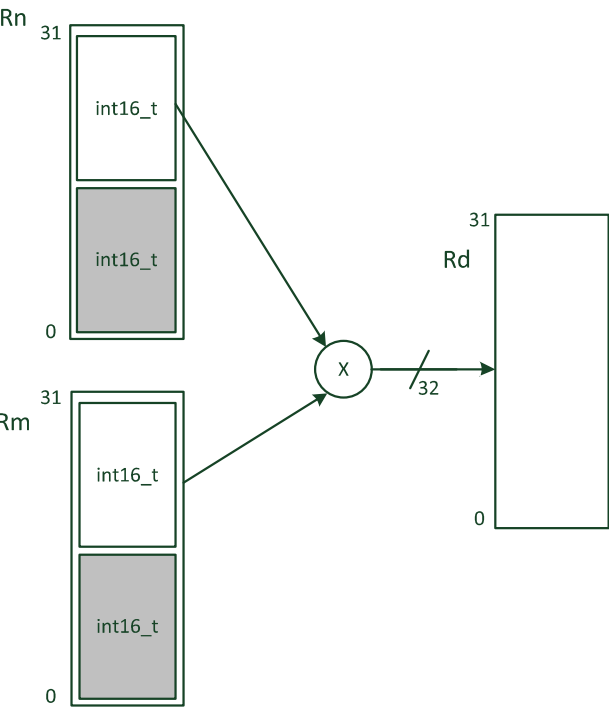


**FIGURE B.29**  
SMULBT



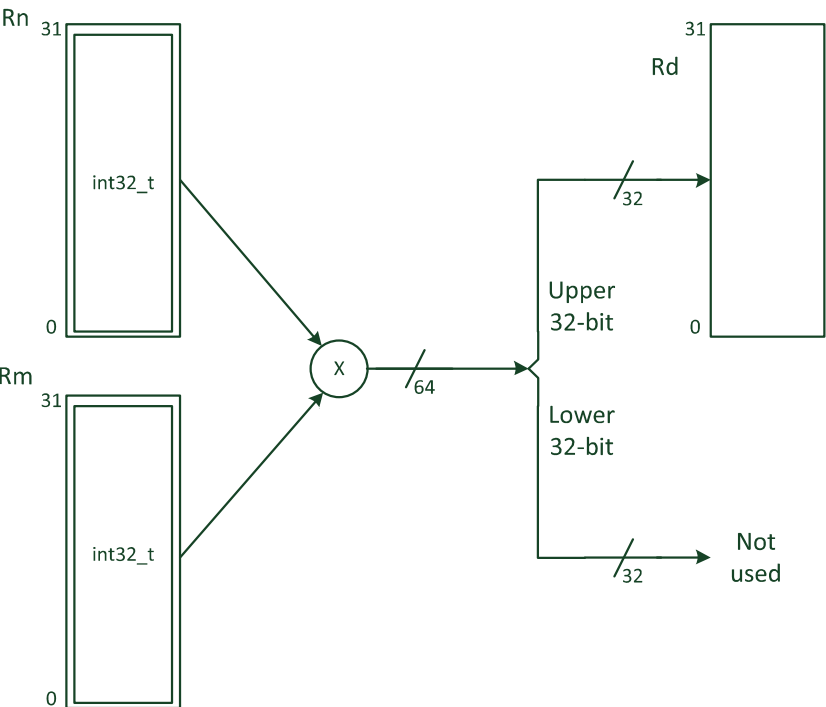
**FIGURE B.30**  
SMULTB

SMULTT {<Rd>,} <Rn>, <Rm>



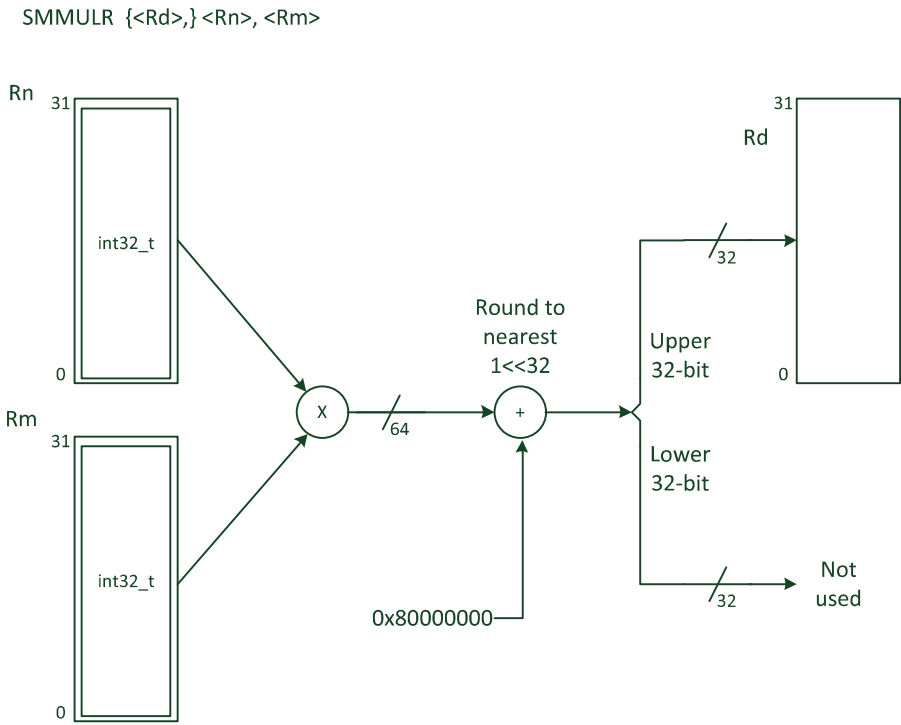
**FIGURE B.31**  
SMULTT

SMMUL {<Rd>,} <Rn>, <Rm>



**FIGURE B.32**  
SMMUL





**FIGURE B.33**  
SMMULR

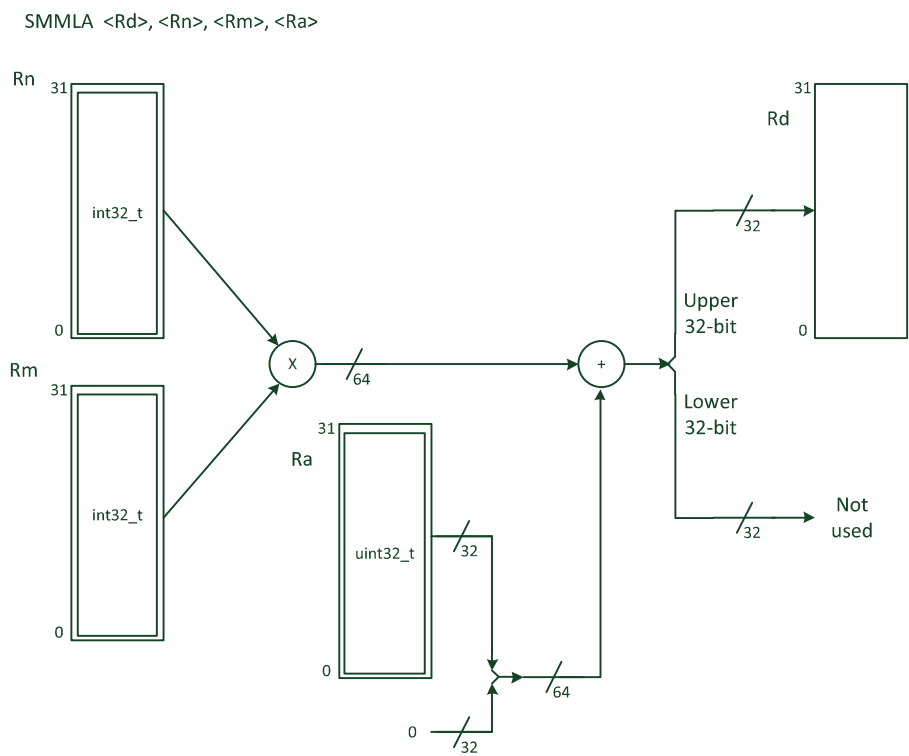
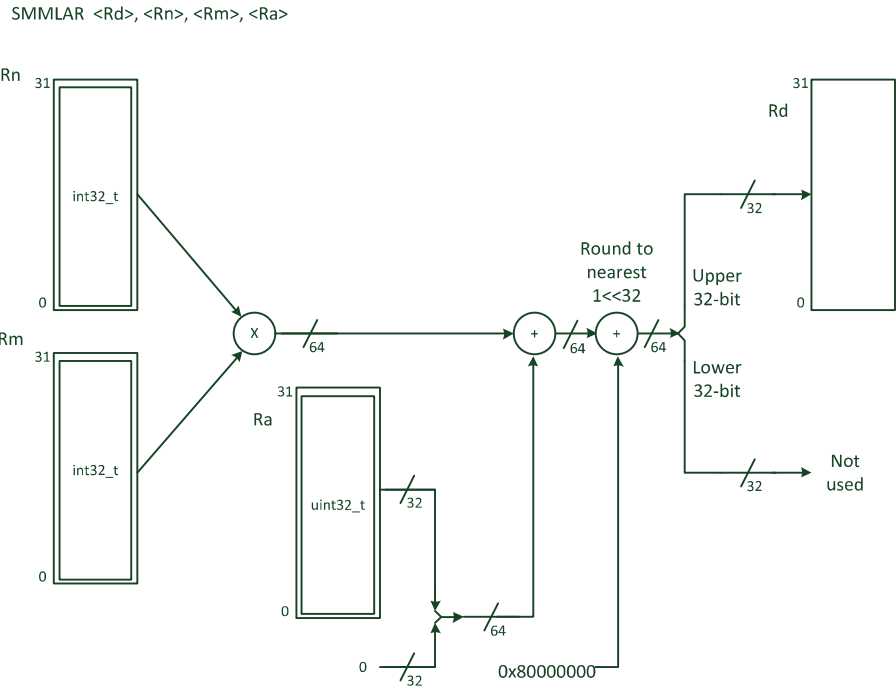
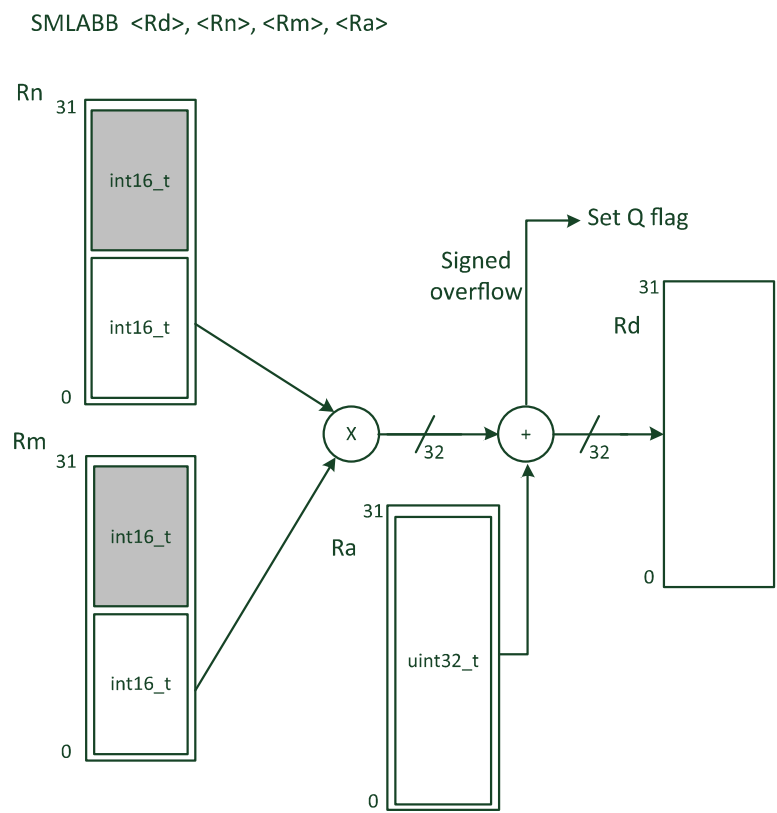


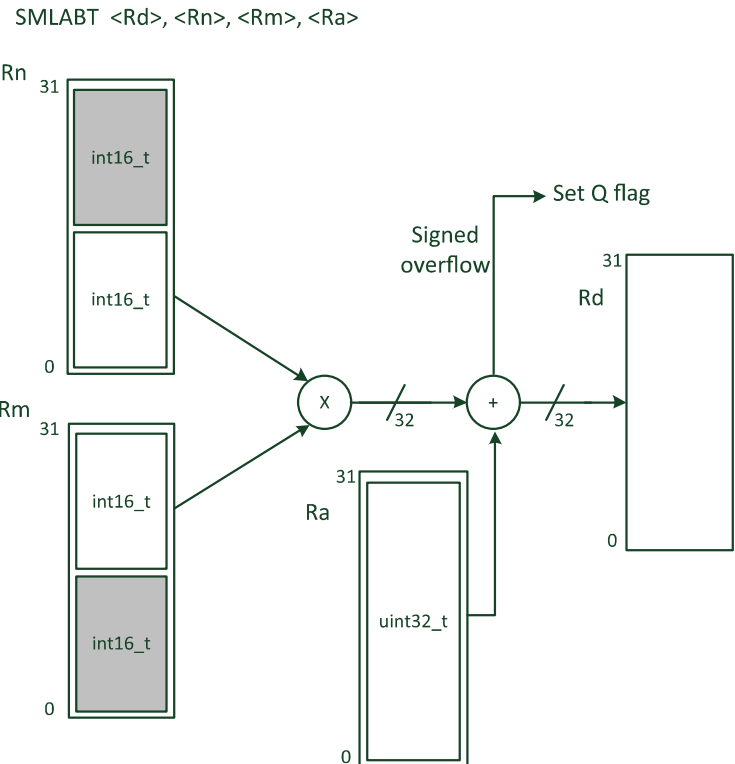
FIGURE B.34  
SMMLA



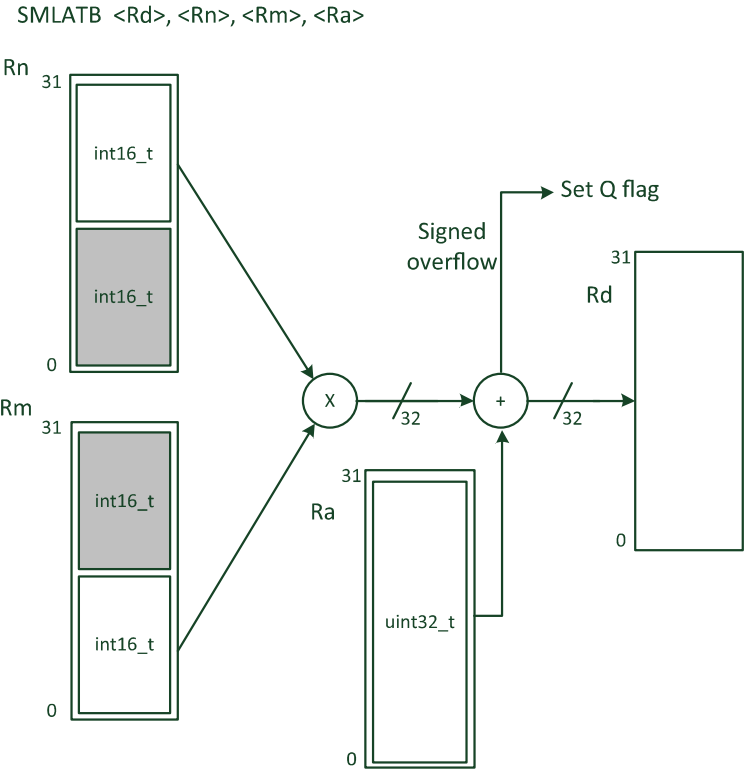
**FIGURE B.35**  
SMMLAR



**FIGURE B.36**  
SMLABB

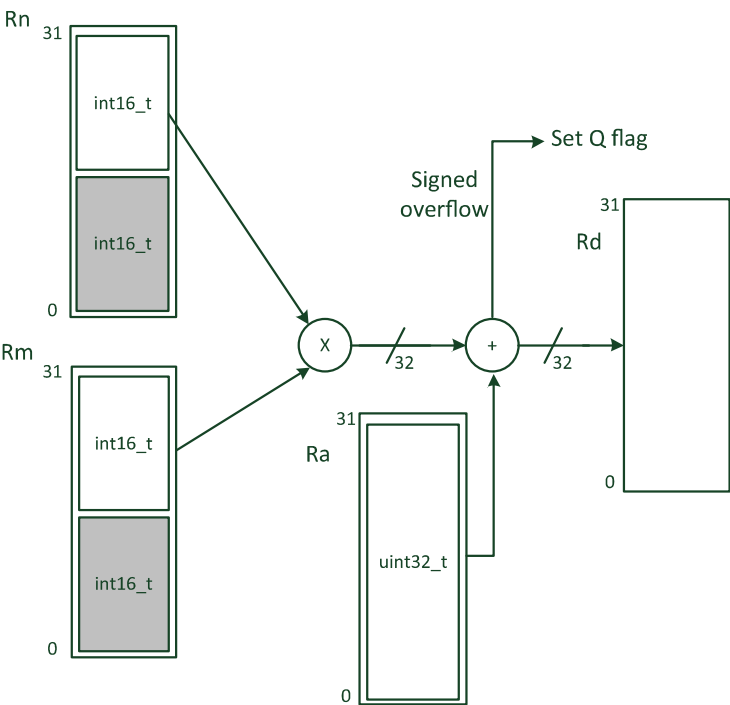


**FIGURE B.37**  
SMLABT

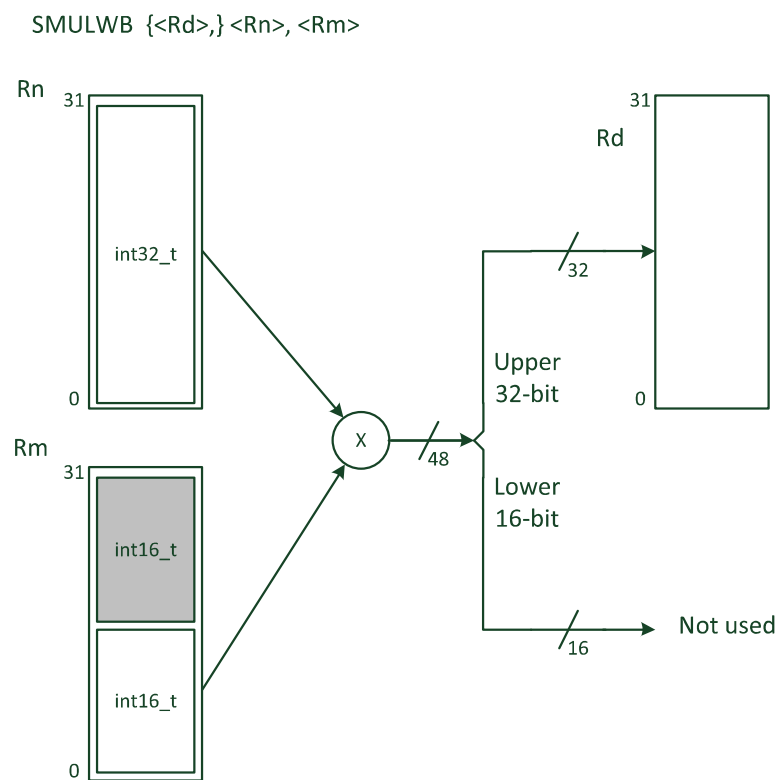


**FIGURE B.38**  
SMLATB

SMLATT <Rd>, <Rn>, <Rm>, <Ra>

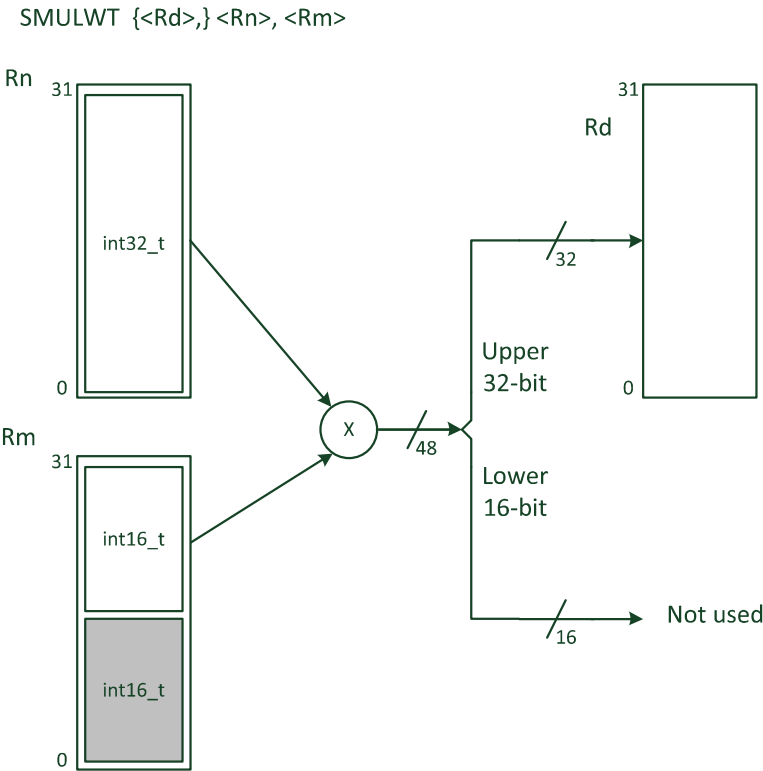


**FIGURE B.39**  
SMLATT



**FIGURE B.40**  
SMULWB





**FIGURE B.41**  
SMULWT

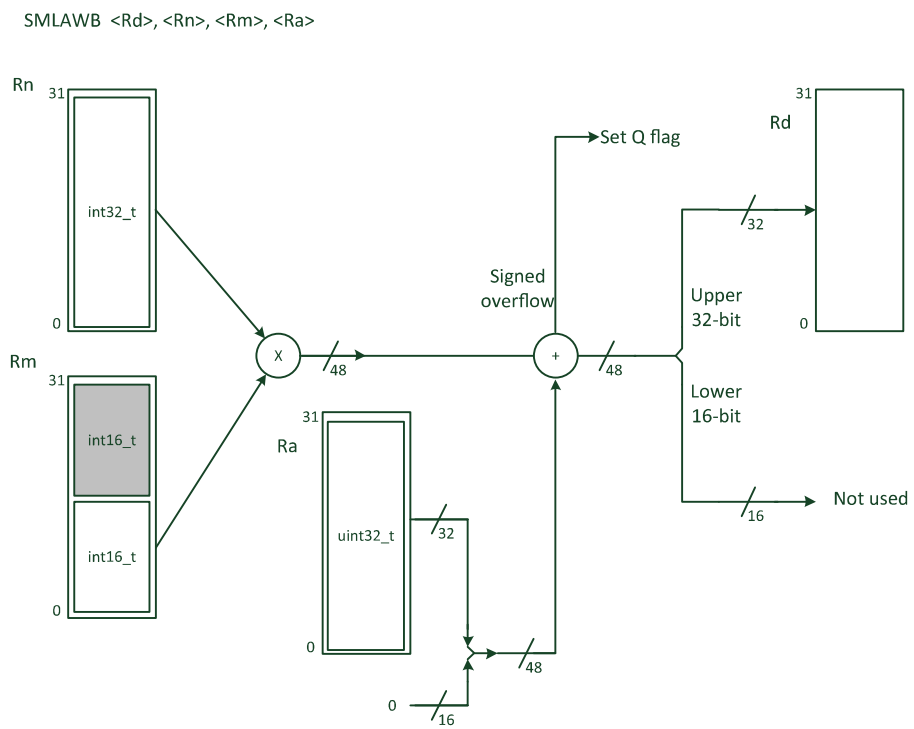
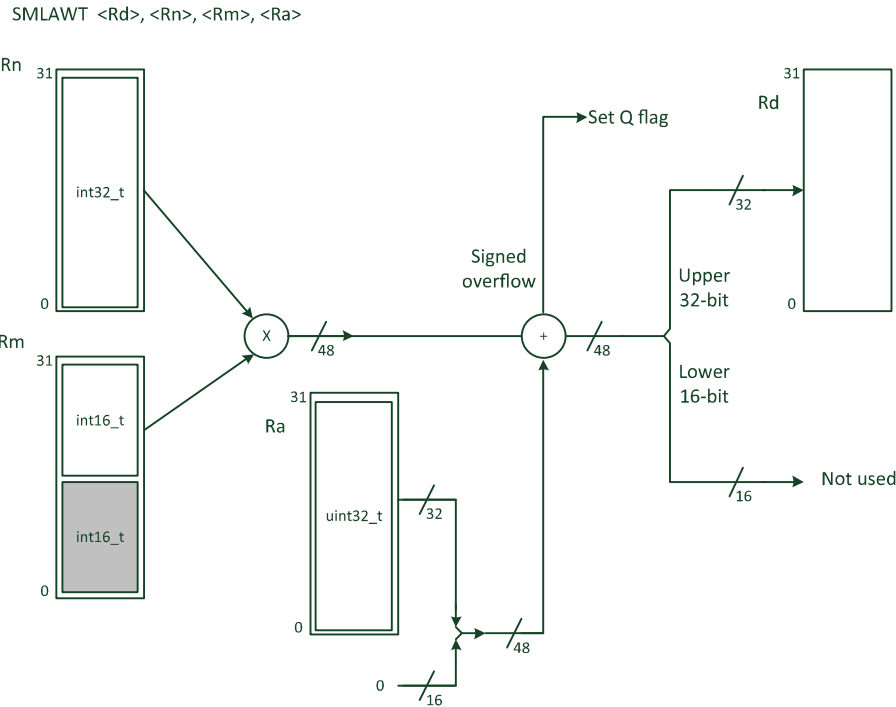
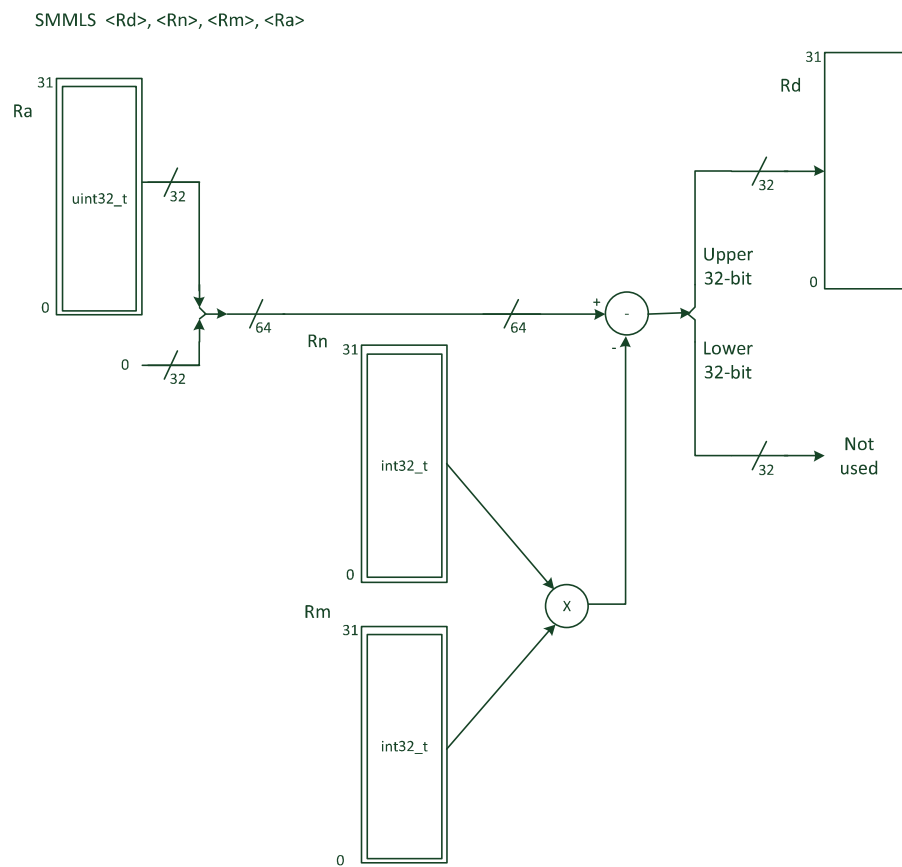


FIGURE B.42

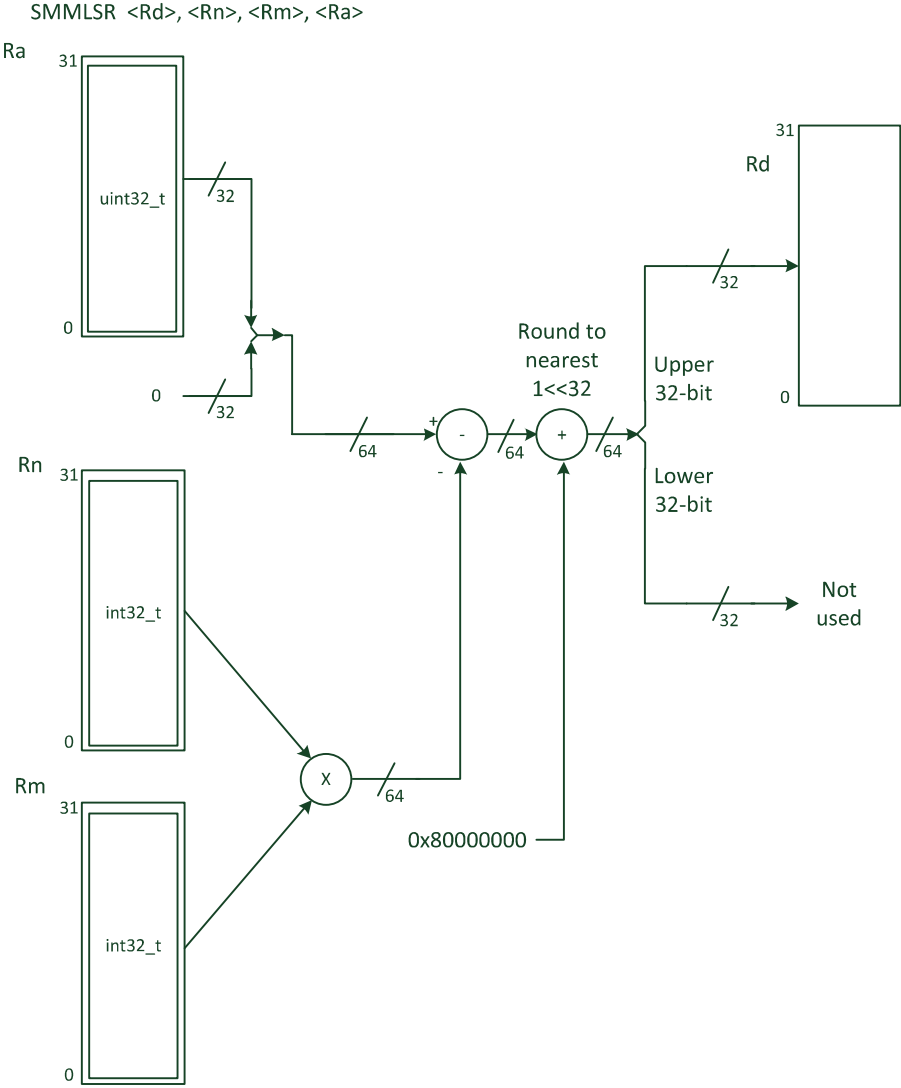
SMLAWB



**FIGURE B.43**  
SMLAWT



**FIGURE B.44**  
SMMLS



**FIGURE B.45**  
SMMLSR

SMLALBB <RdLo>, <RdHi>, <Rn>, <Rm>

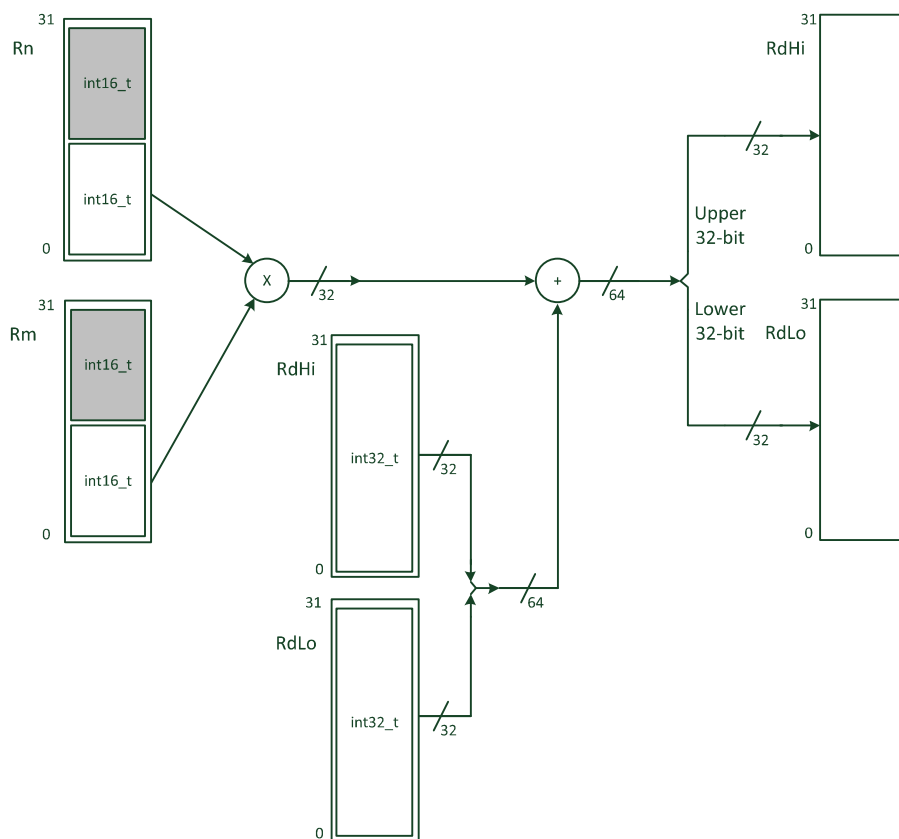
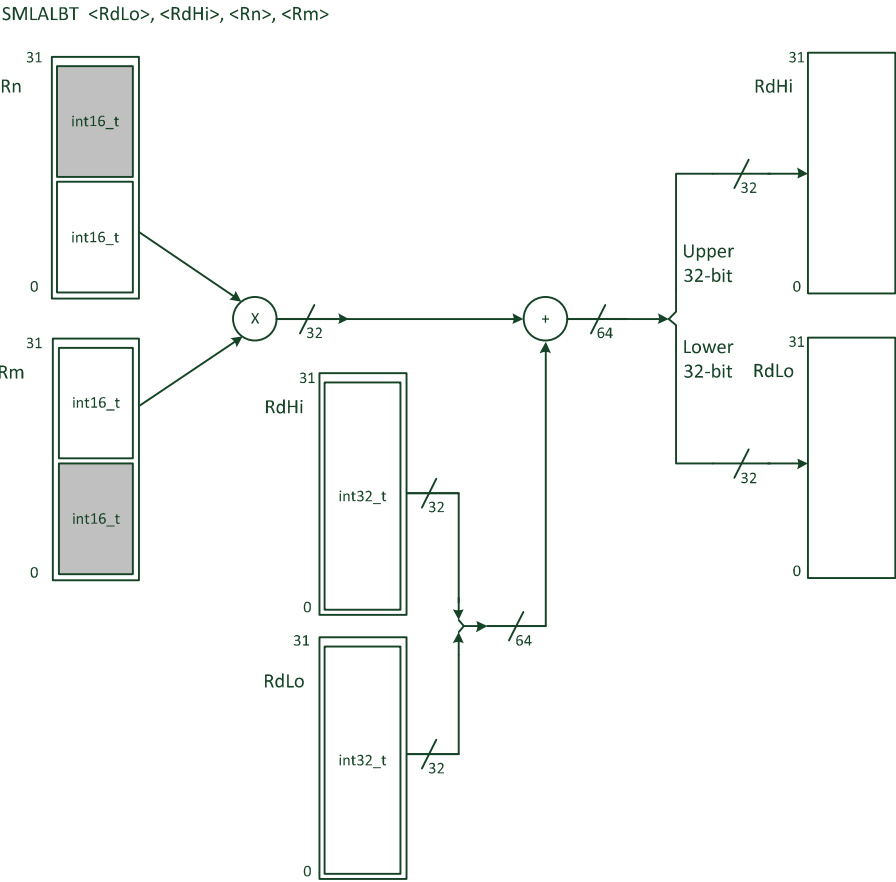


FIGURE B.46

SMLALBB



**FIGURE B.47**  
SMLALBT

SMLALTB <RdLo>, <RdHi>, <Rn>, <Rm>

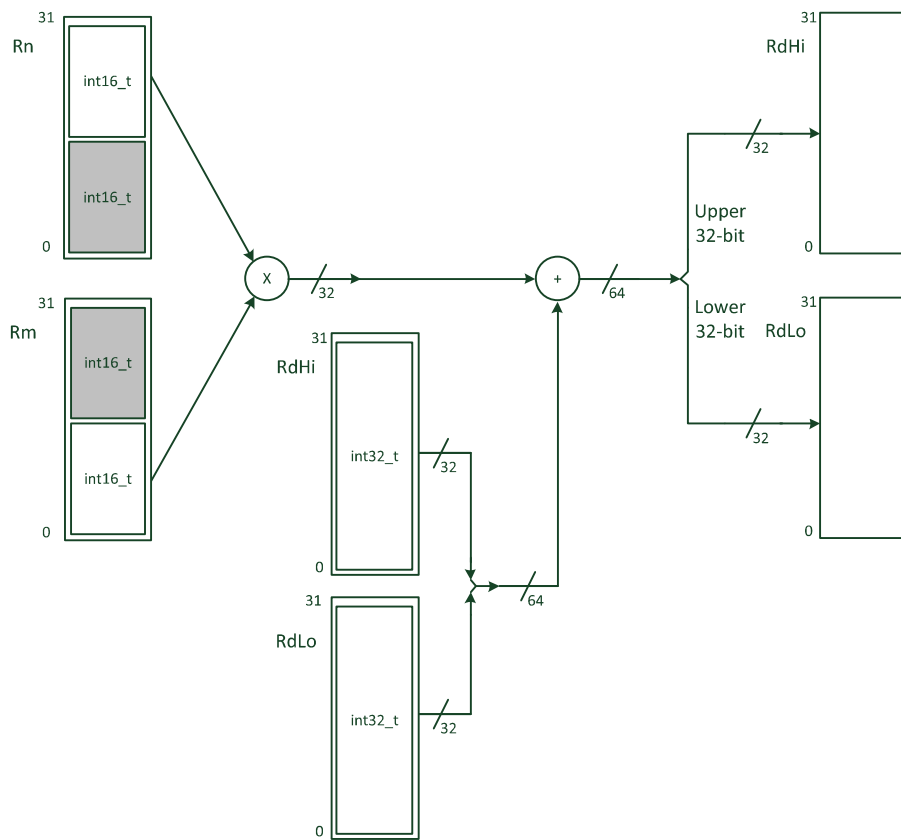
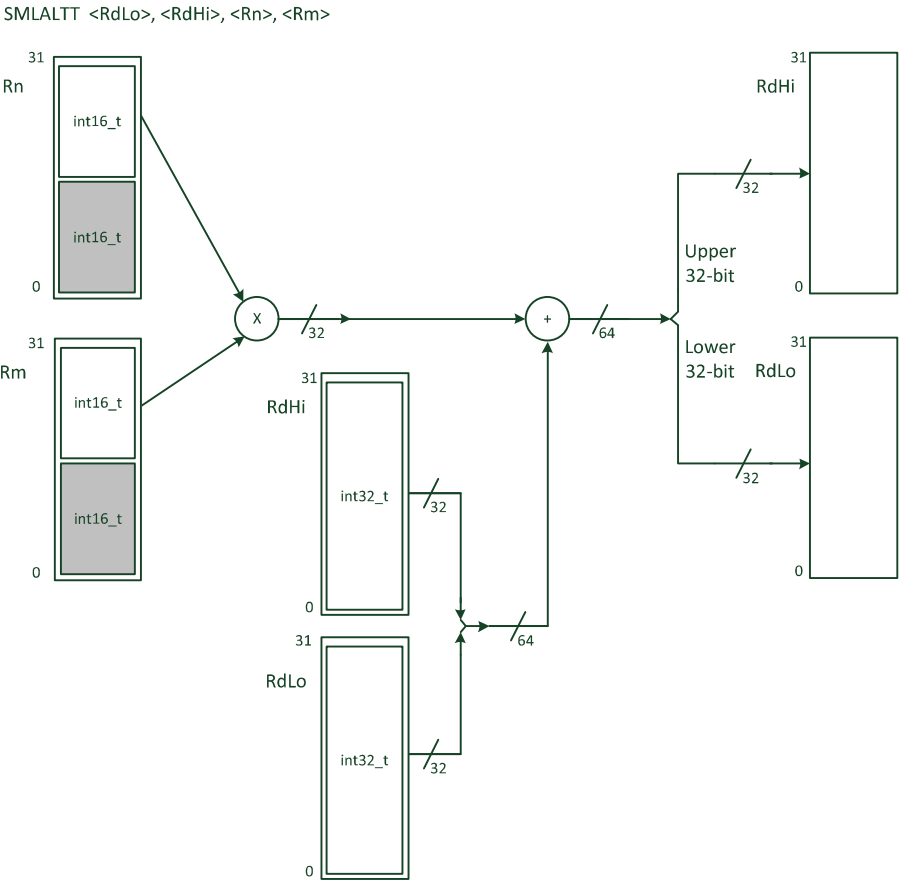


FIGURE B.48

SMLALTB





**FIGURE B.49**  
SMLALTT

SMUAD {<Rd>}, <Rn>, <Rm>

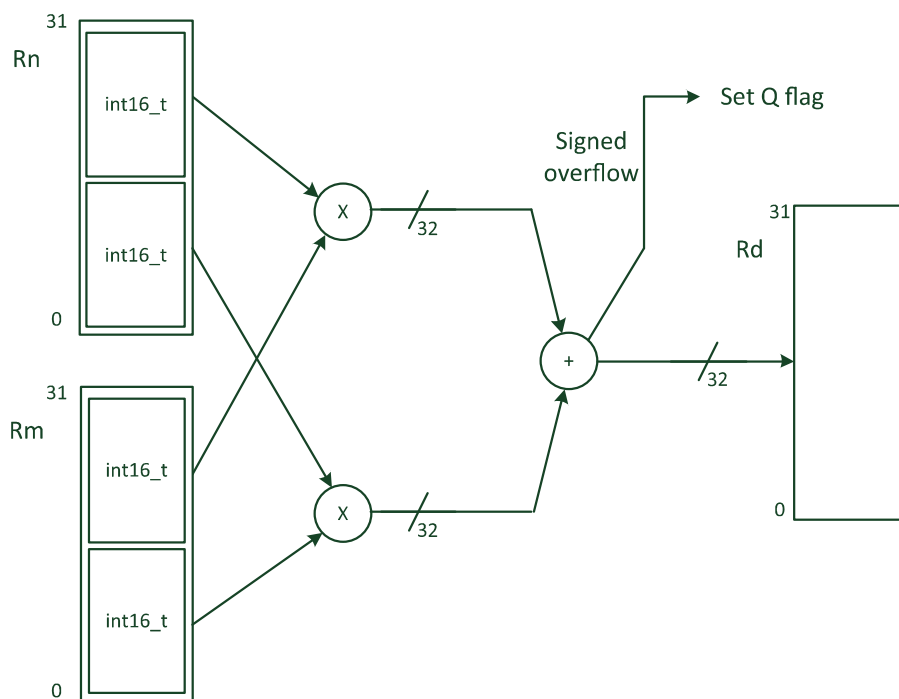
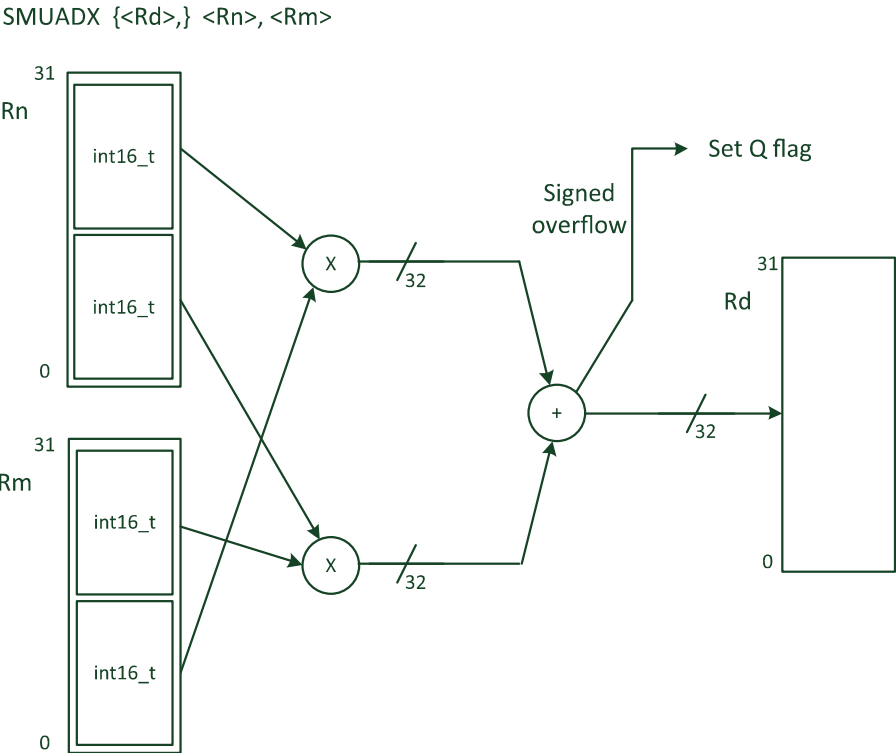


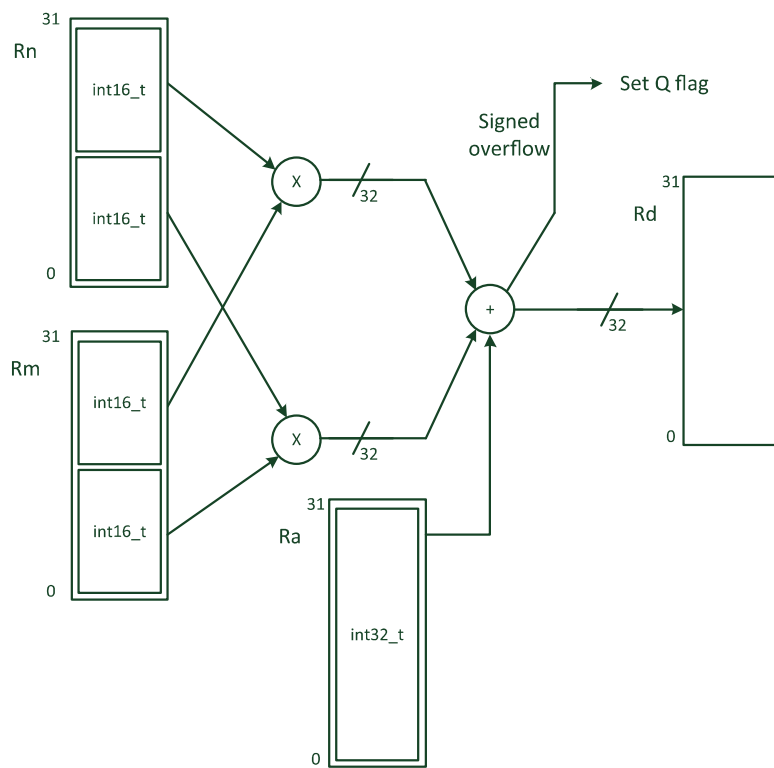
FIGURE B.50

SMUAD



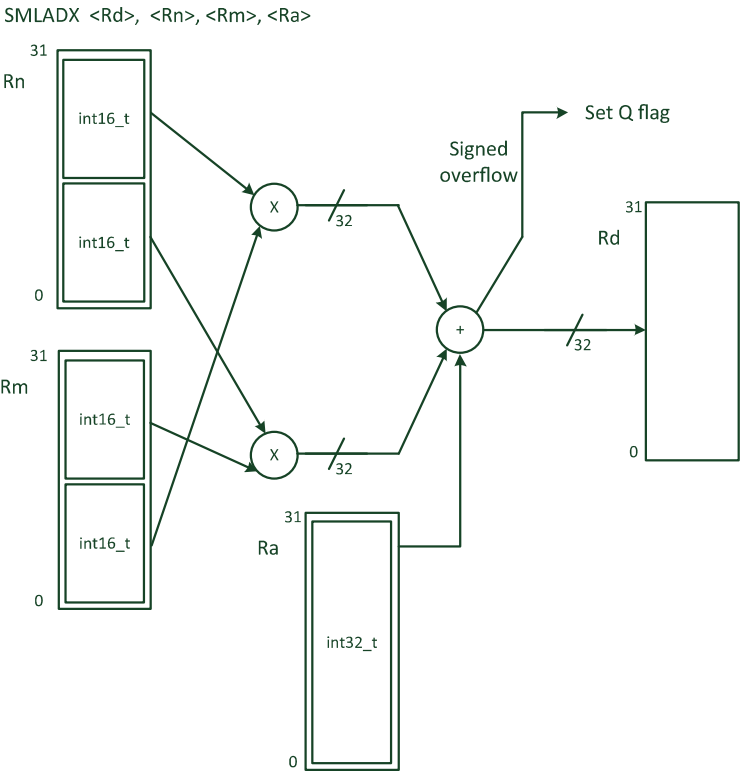
**FIGURE B.51**  
SMUADX

SMLAD <Rd>, <Rn>, <Rm>, <Ra>



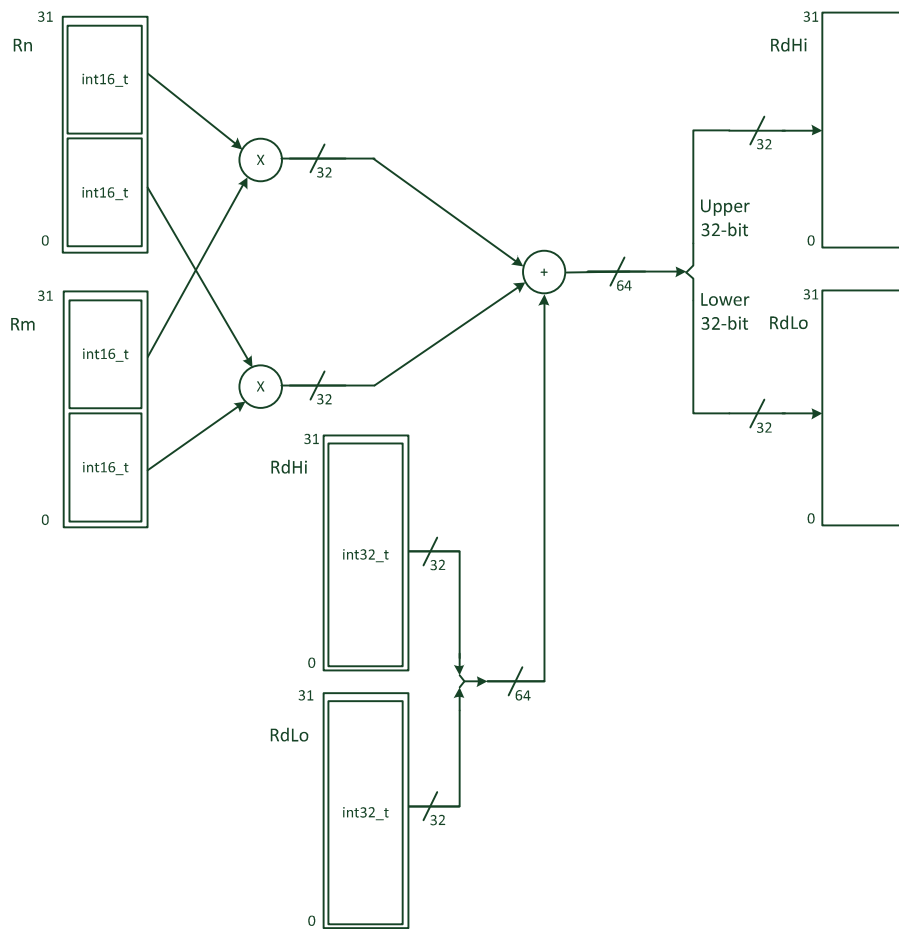
**FIGURE B.52**

SMLAD



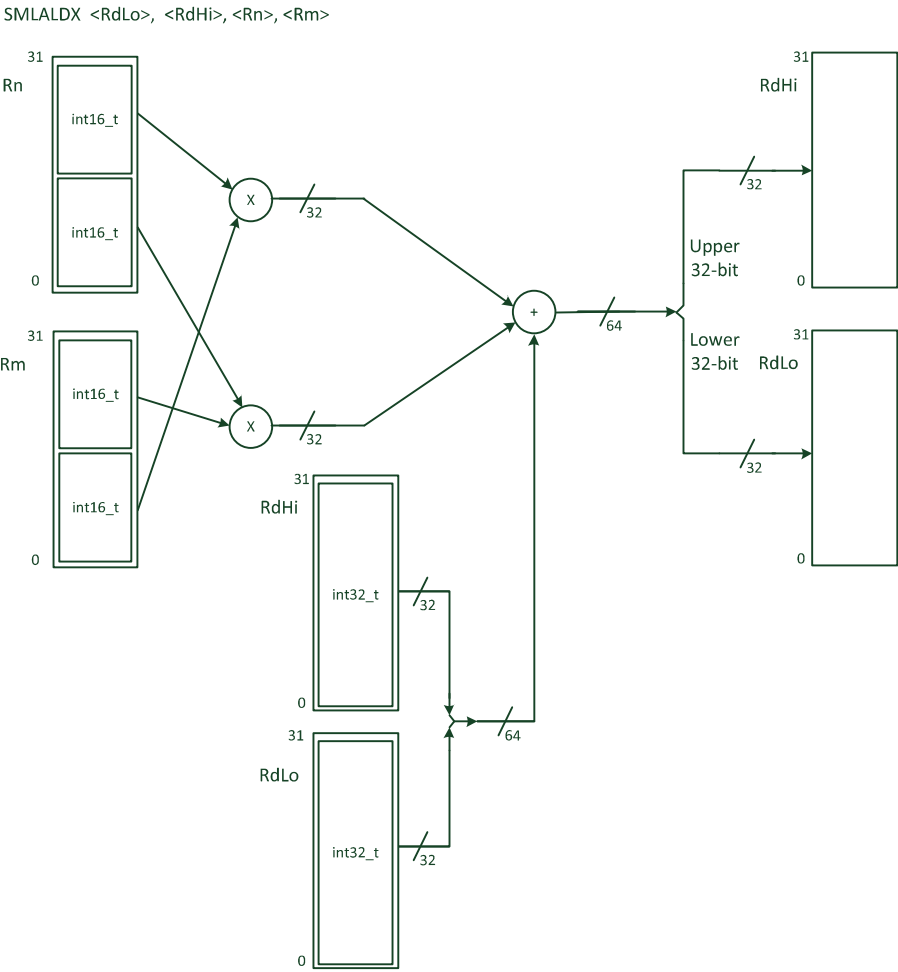
**FIGURE B.53**  
SMLADX

SMLALD <RdLo>, <RdHi>, <Rn>, <Rm>



**FIGURE B.54**

SMLALD



**FIGURE B.55**  
SMLALX

SMUSD {<Rd>,} <Rn>, <Rm>

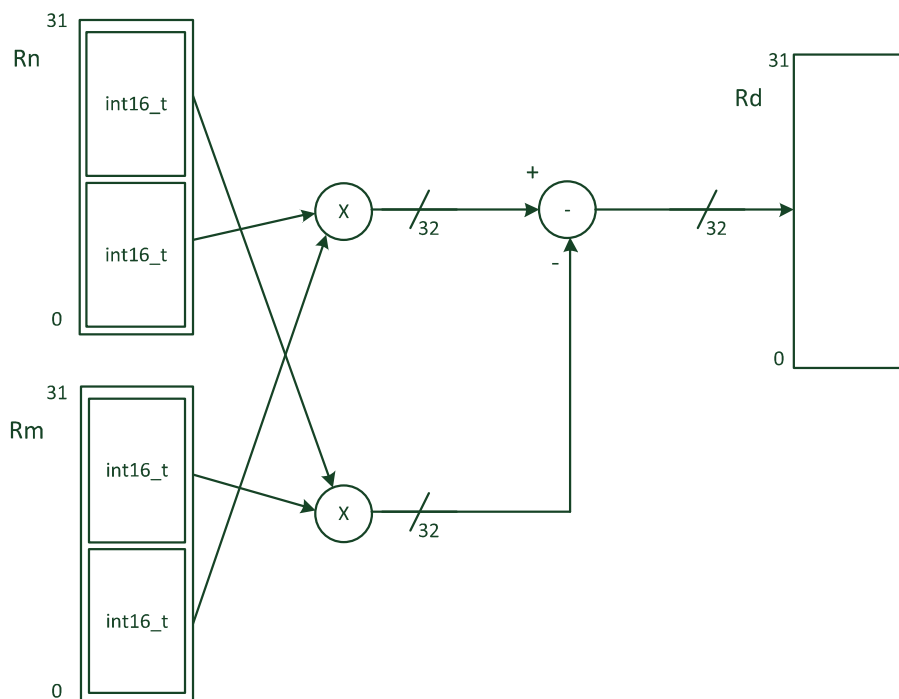
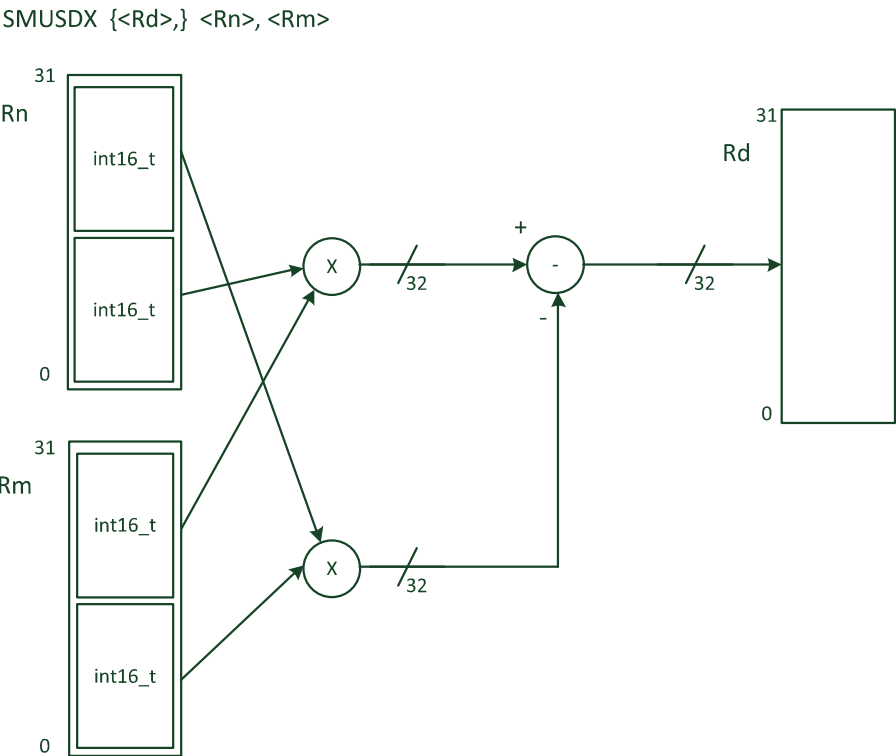


FIGURE B.56

SMUSD





**FIGURE B.57**  
SMUSD<sub>X</sub>

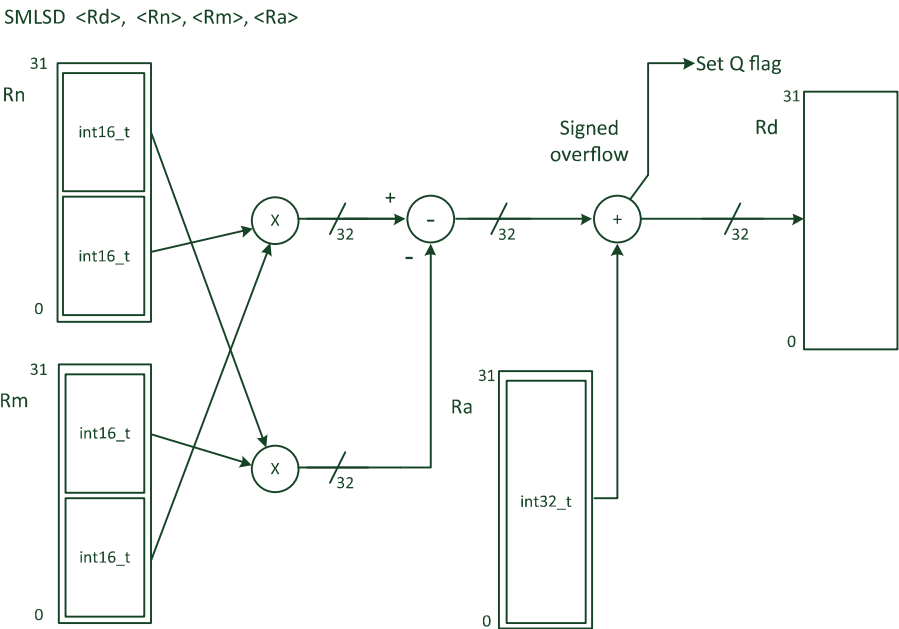
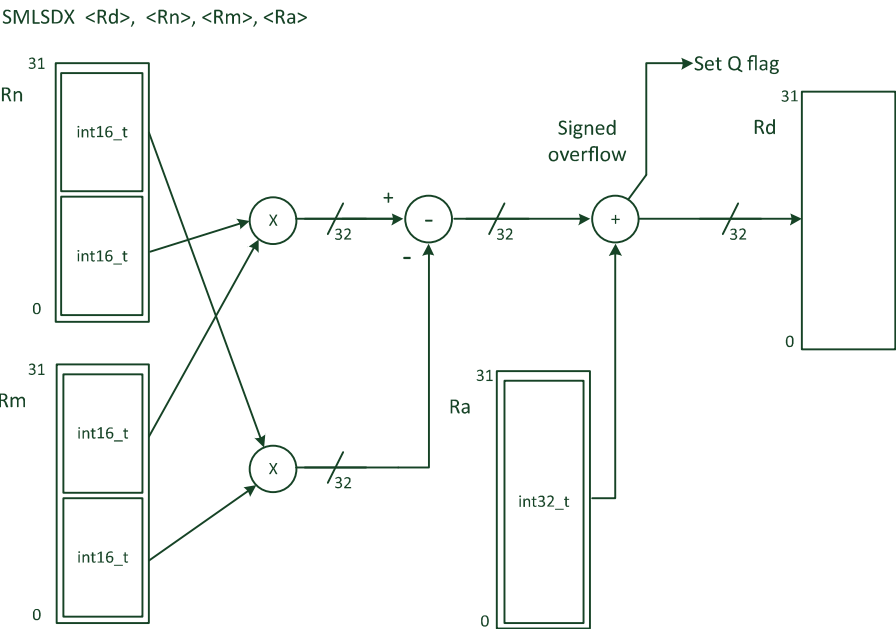


FIGURE B.58

SMLSD



**FIGURE B.59**  
SMLSDX

SMLS LD <RdLo>, <RdHi>, <Rn>, <Rm>

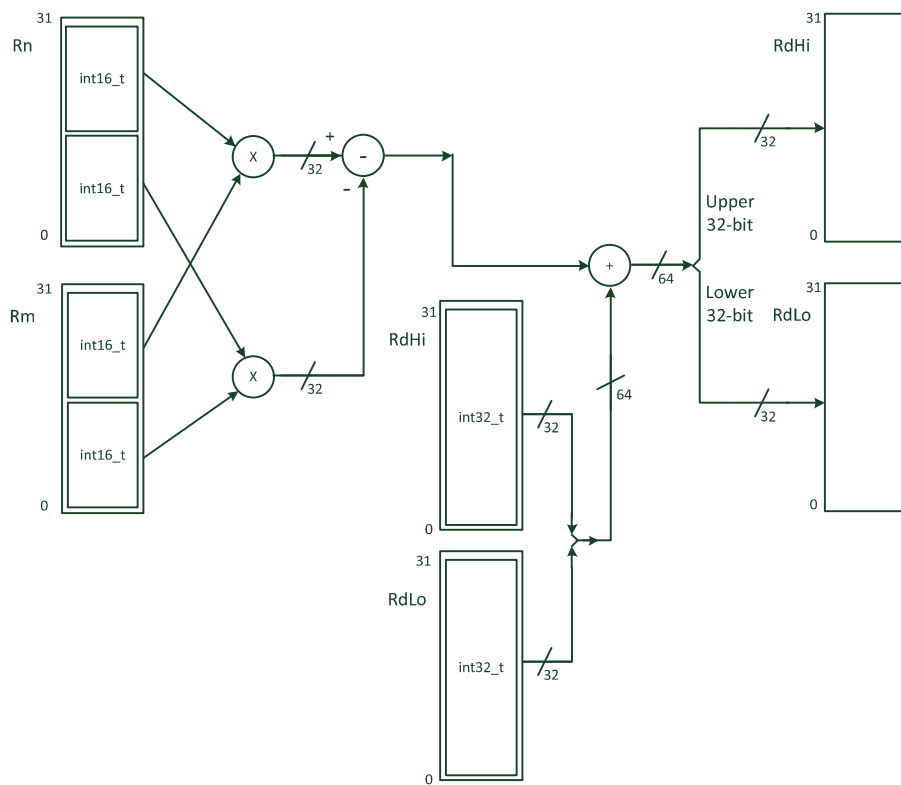
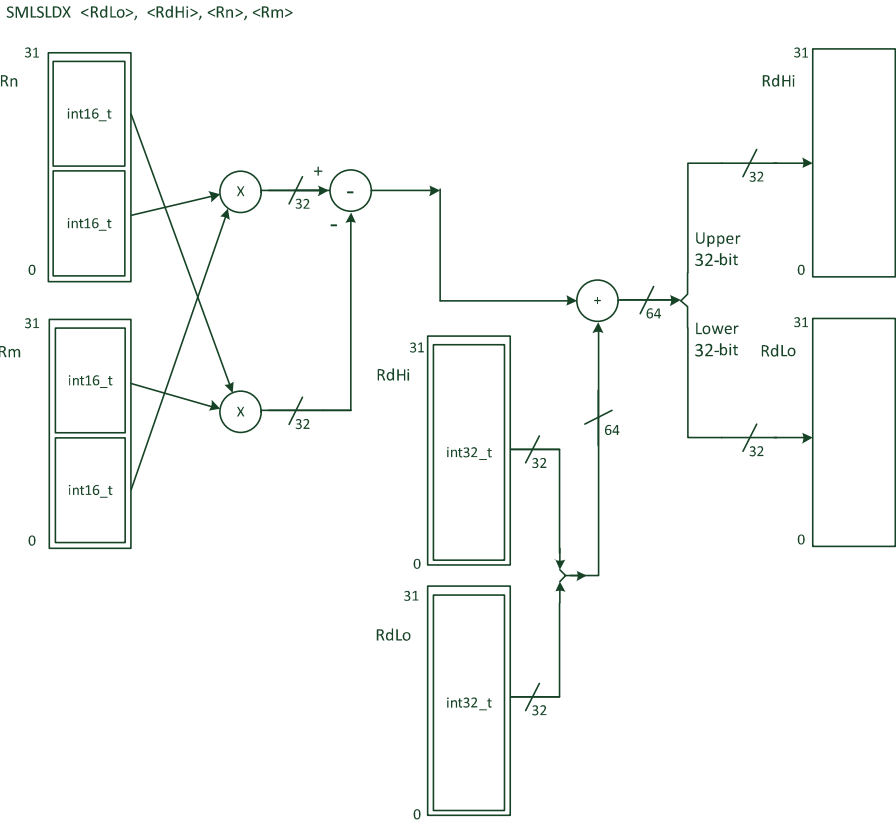


FIGURE B.60

SMLS LD



**FIGURE B.61**  
SMLSLDX

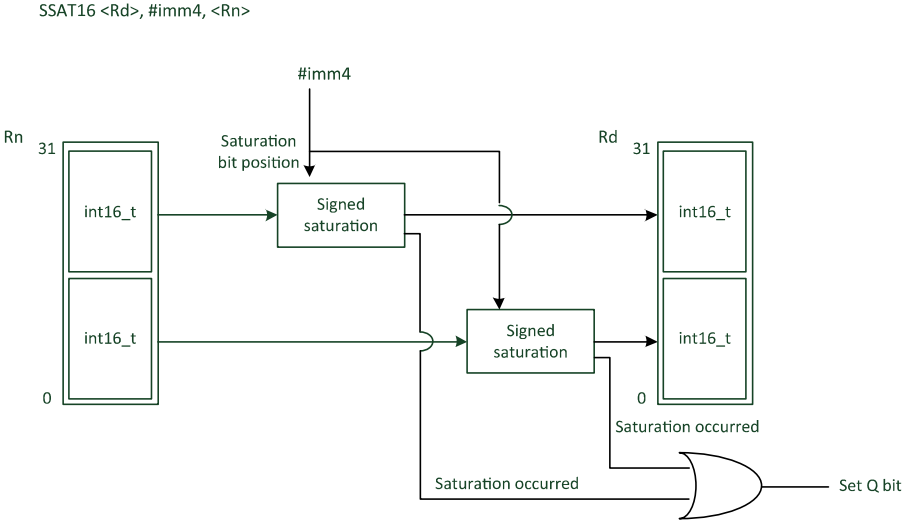


FIGURE B.62

SSAT16

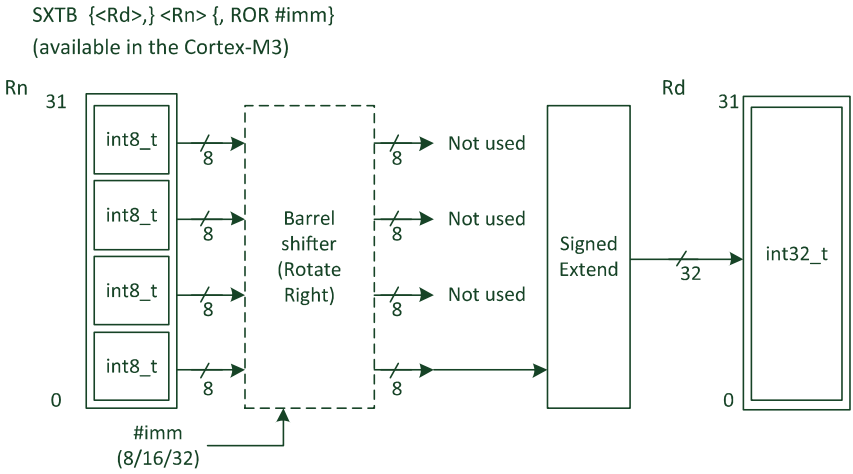


FIGURE B.63

SXTB

SXTB16 {<Rd>}, <Rn> {, ROR #imm}

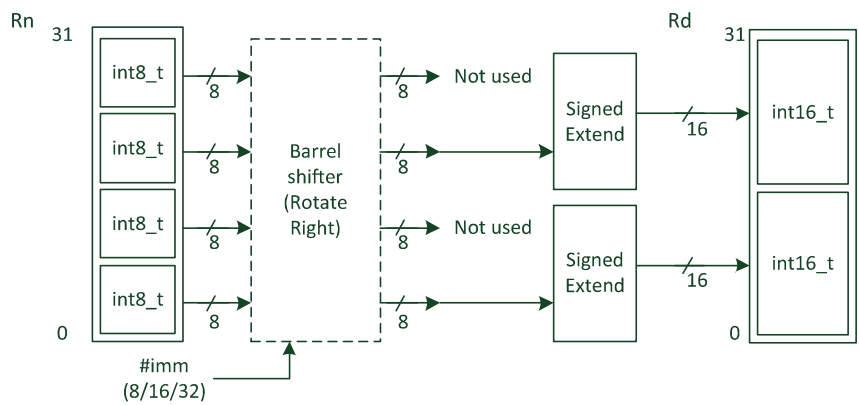


FIGURE B.64

SXTB16

SXTAB {<Rd>}, <Rn>, <Rm> {, ROR #imm}

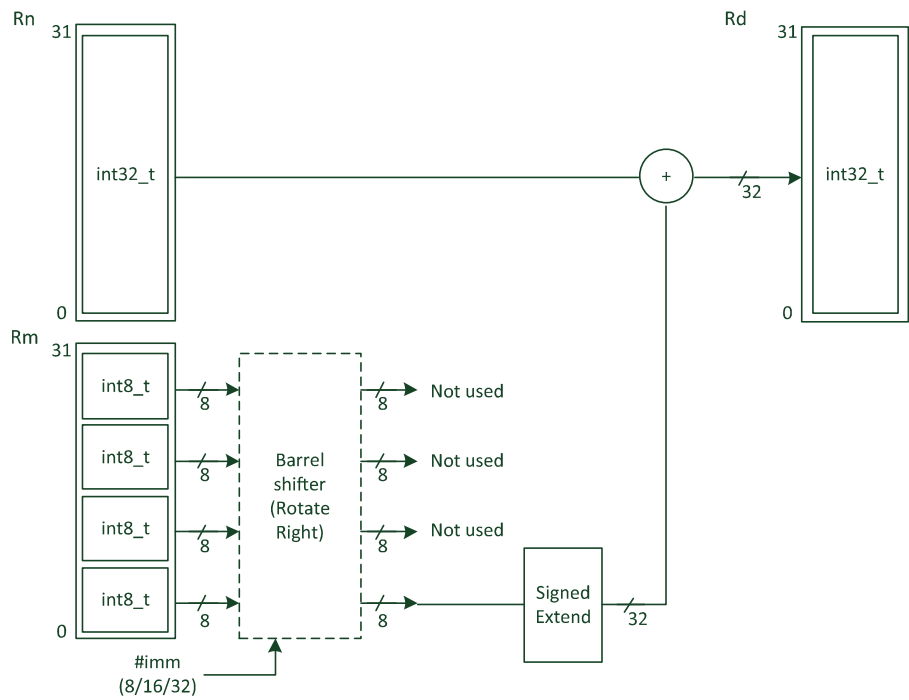


FIGURE B.65

SXTAB

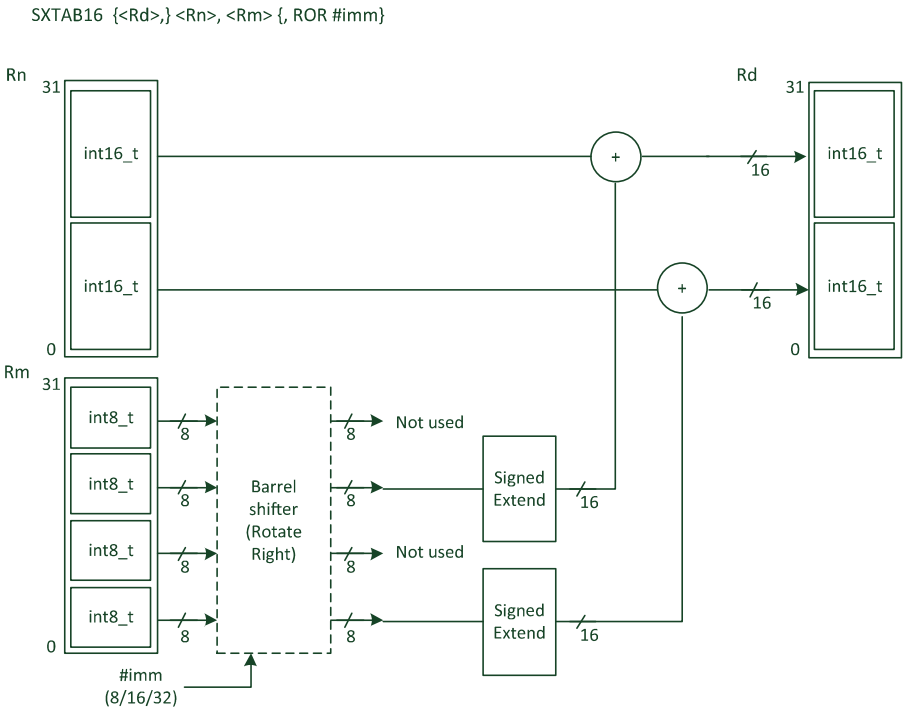


FIGURE B.66

SXTAB16

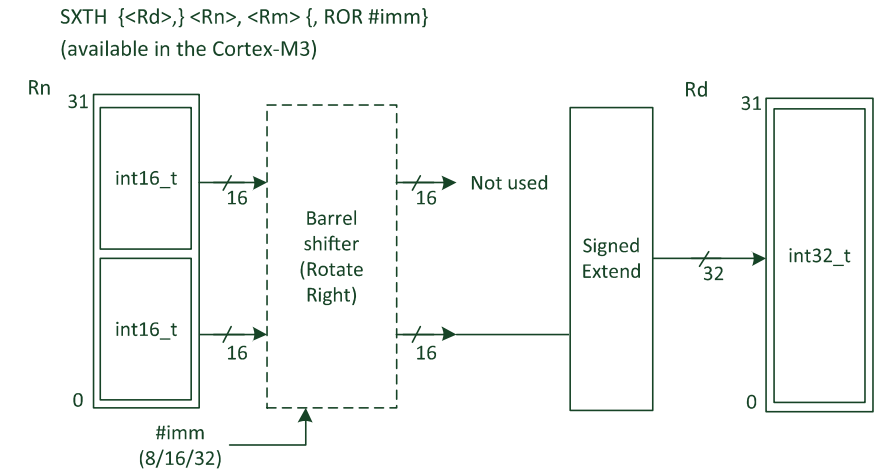


FIGURE B.67

SXTH



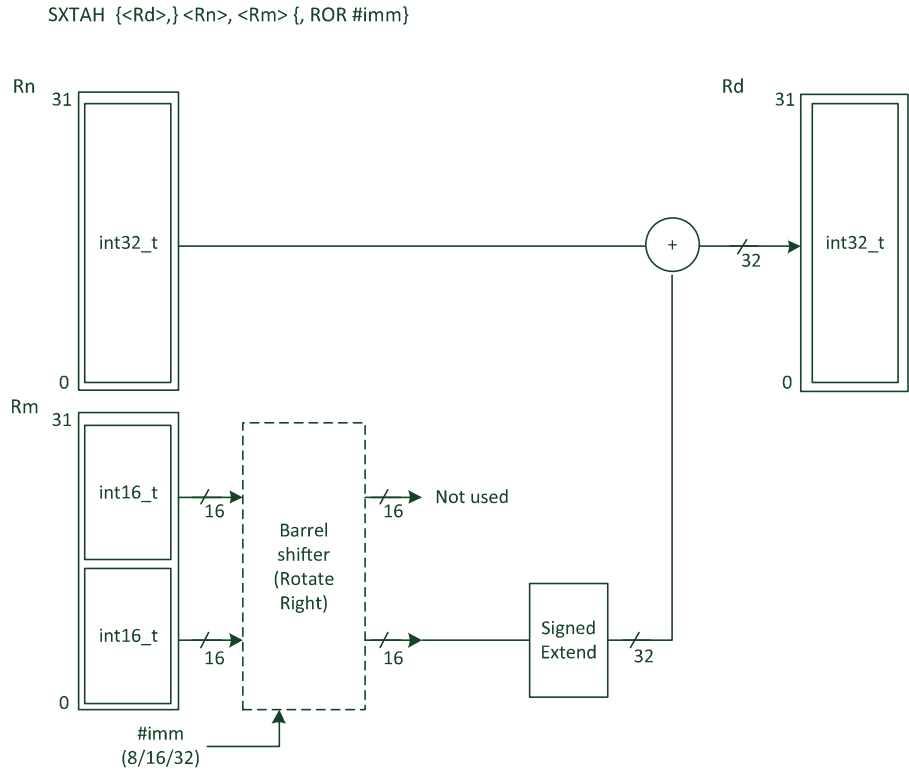


FIGURE B.68

SXTAH

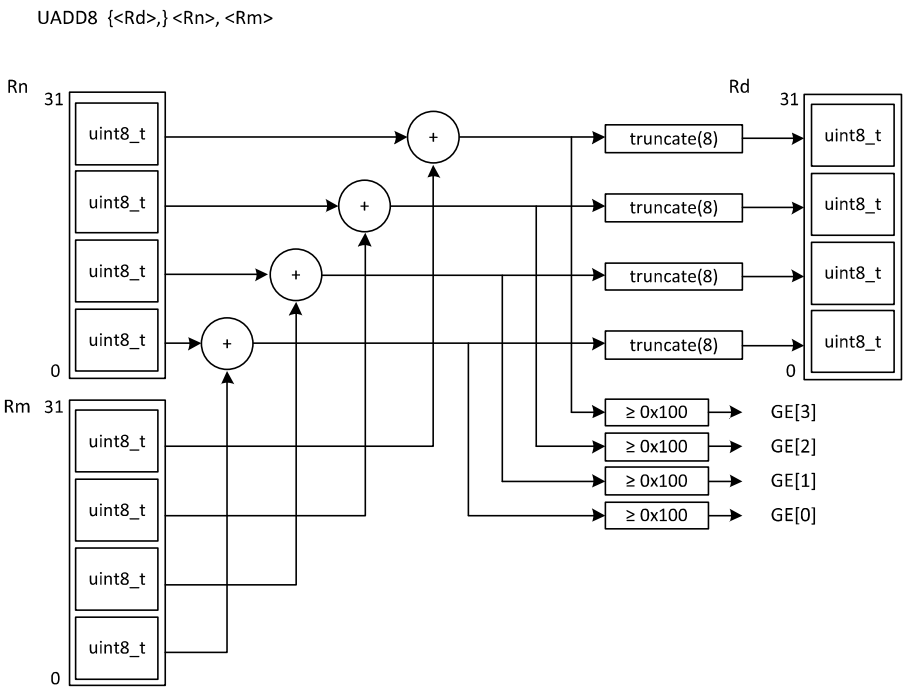
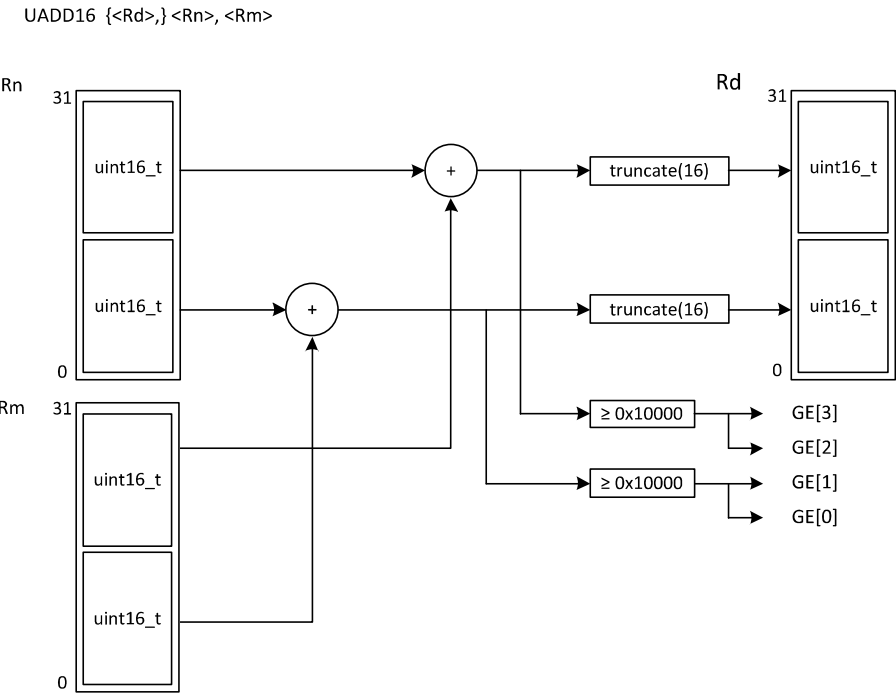
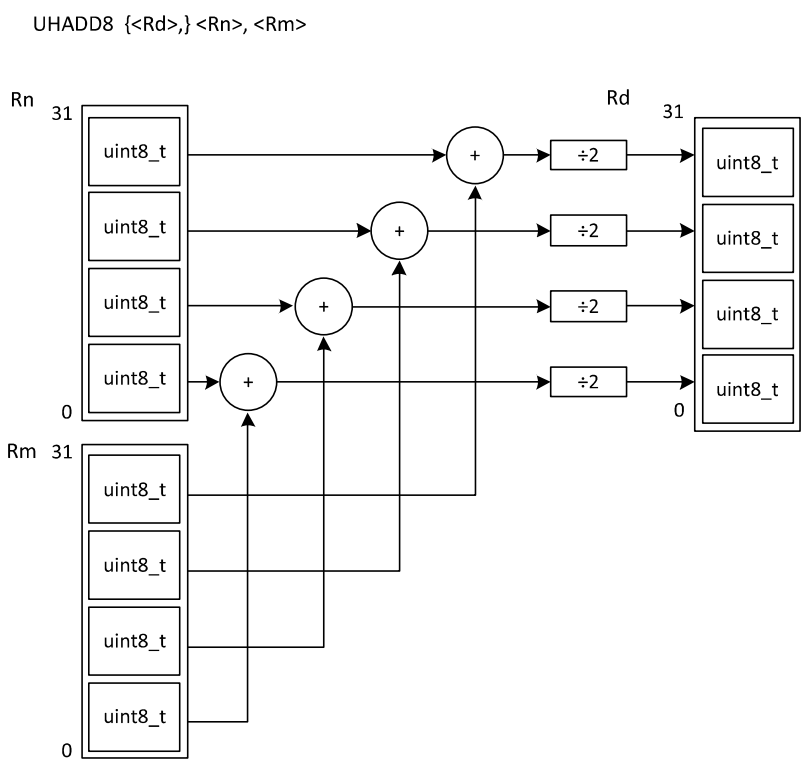


FIGURE B.69

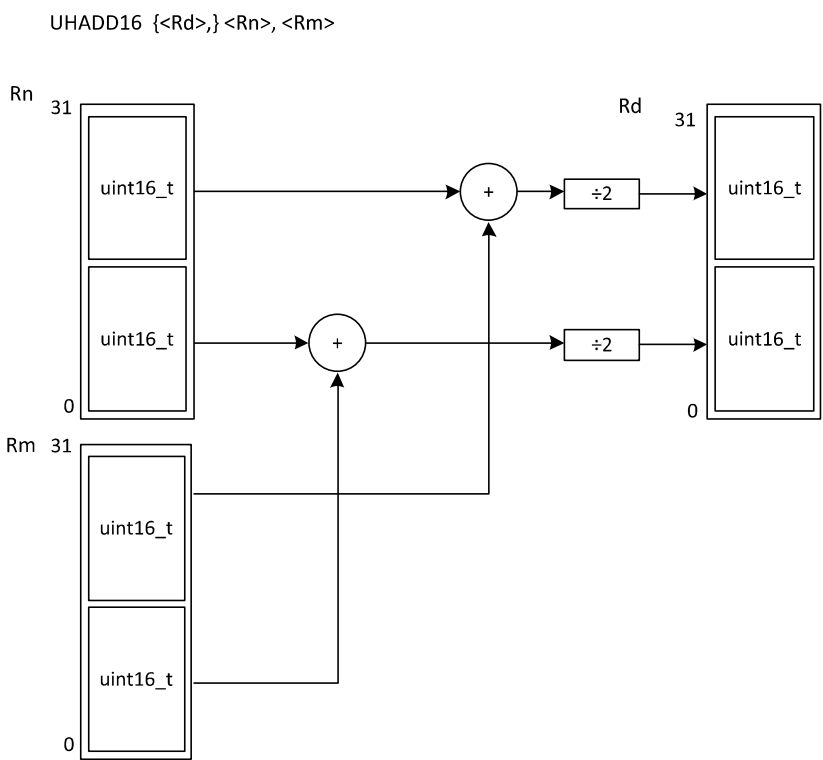
UADD8



**FIGURE B.70**  
UADD16



**FIGURE B.71**  
UHADD8



**FIGURE B.72**  
UHADD16

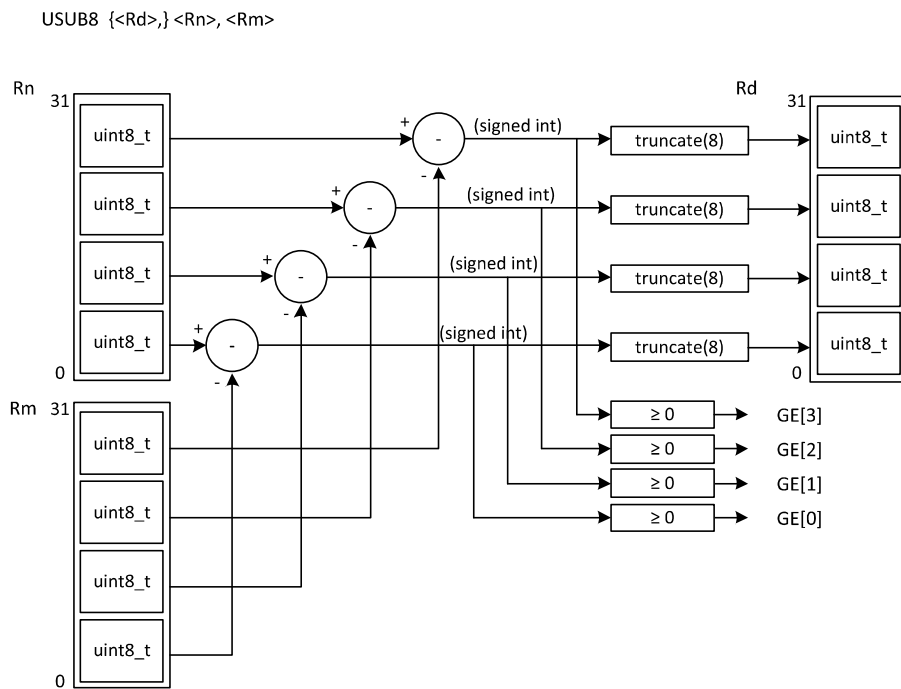


FIGURE B.73

USUB8

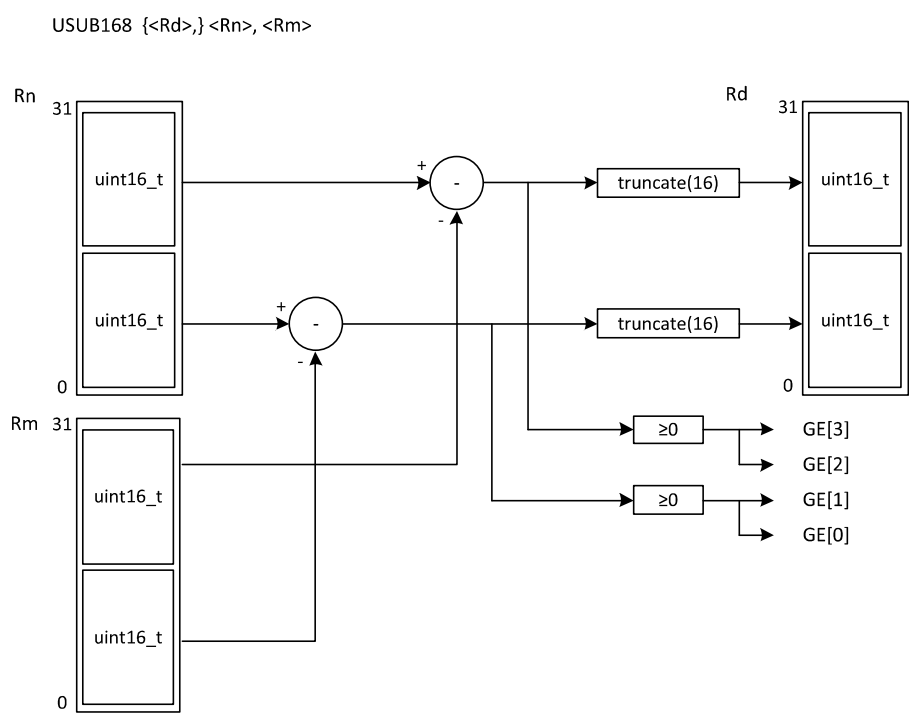


FIGURE B.74

USUB16

UHSUB8 {<Rd>,} <Rn>, <Rm>

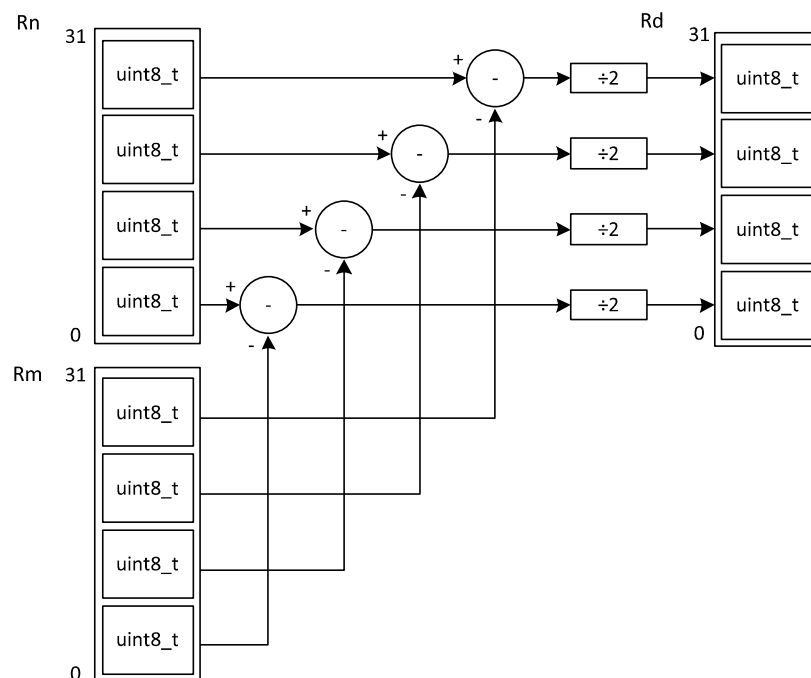
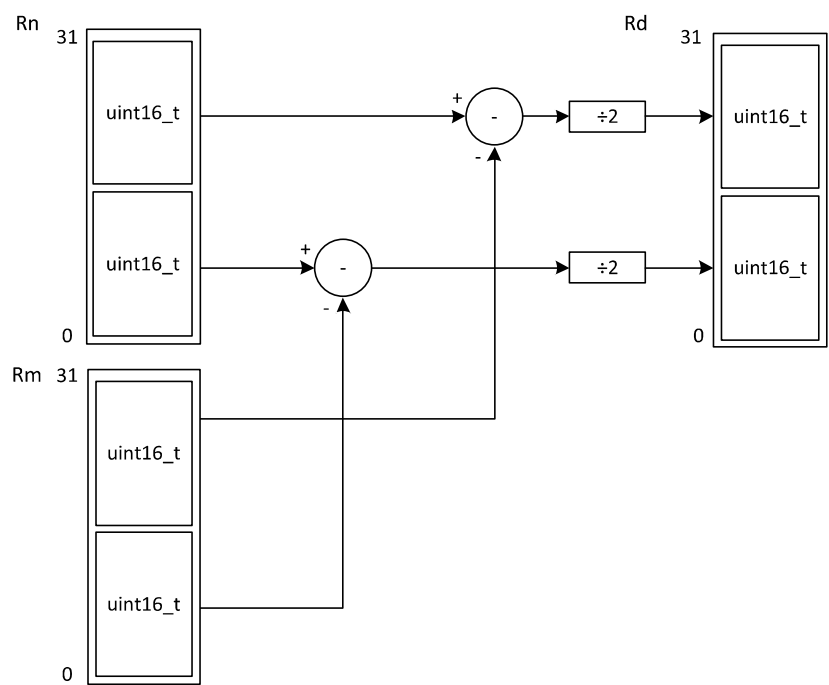


FIGURE B.75

UHSUB8



UHSUB16 {<Rd>}, <Rn>, <Rm>



**FIGURE B.76**  
UHSUB16

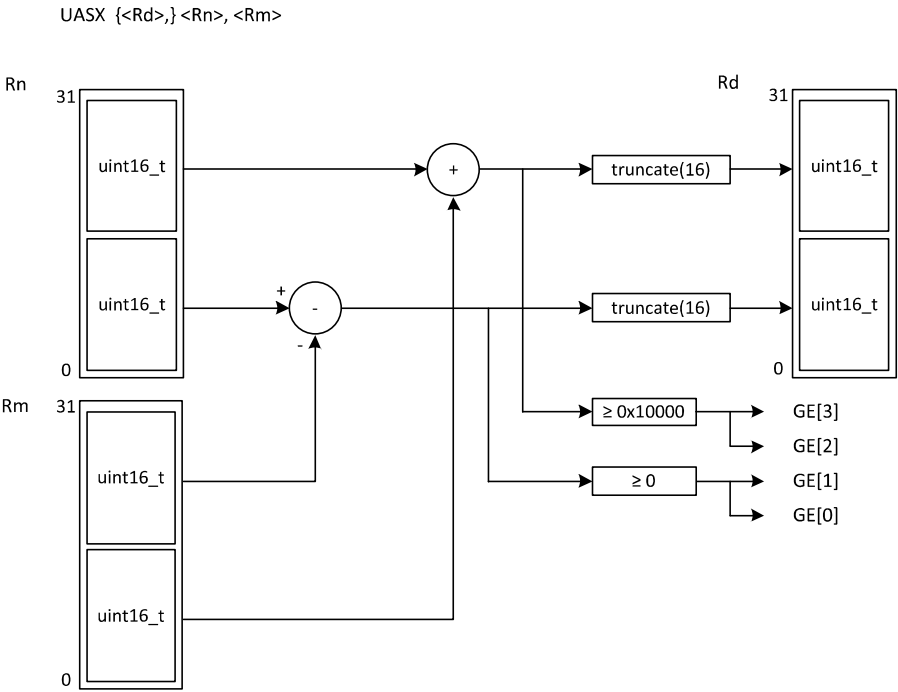


FIGURE B.77

UASX

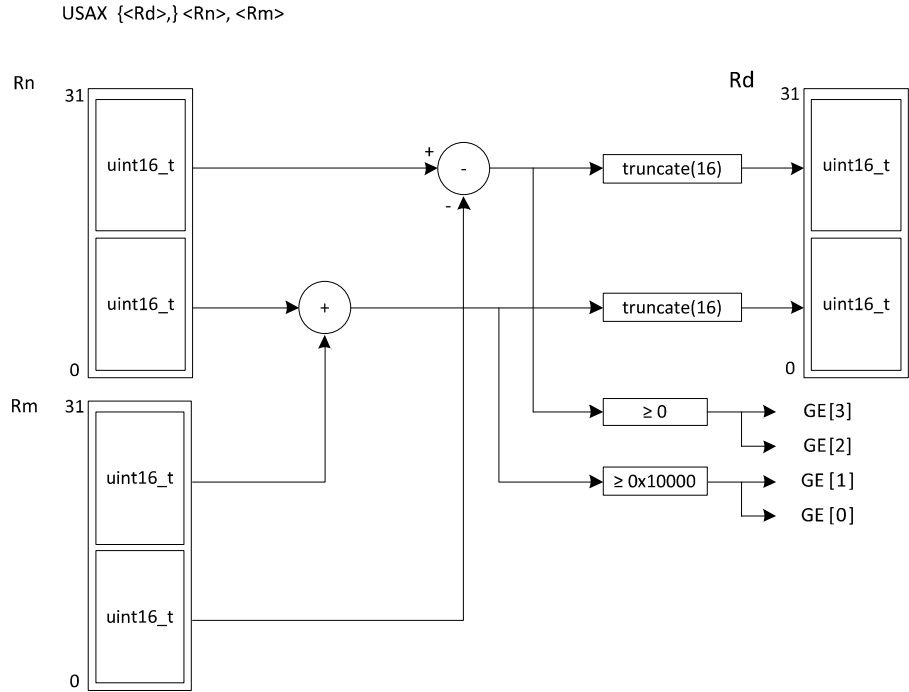
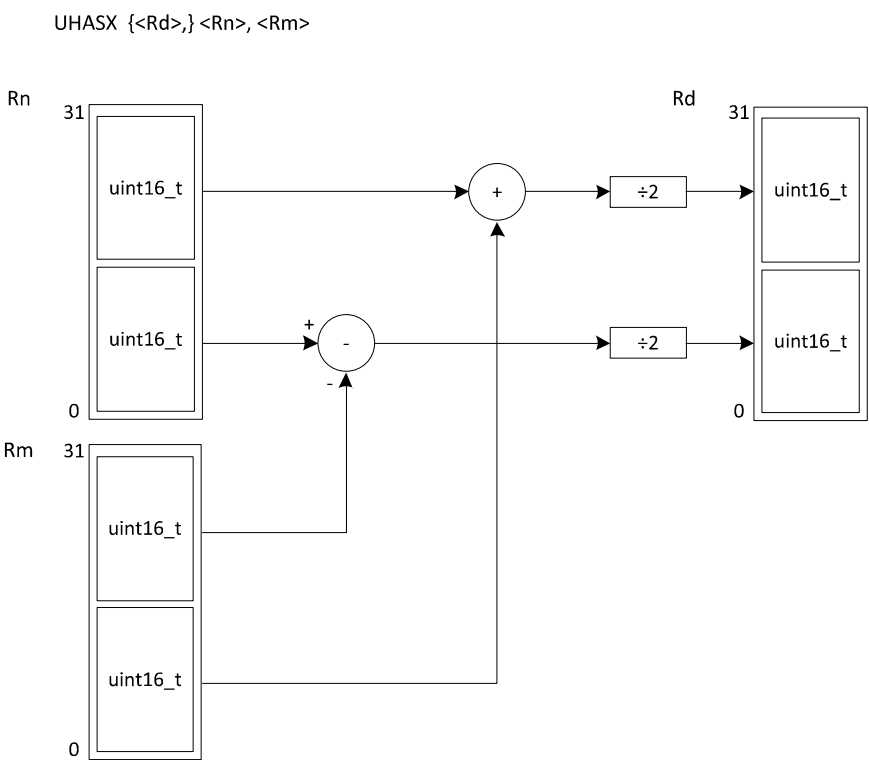


FIGURE B.78

USAX



**FIGURE B.79**  
UHASX

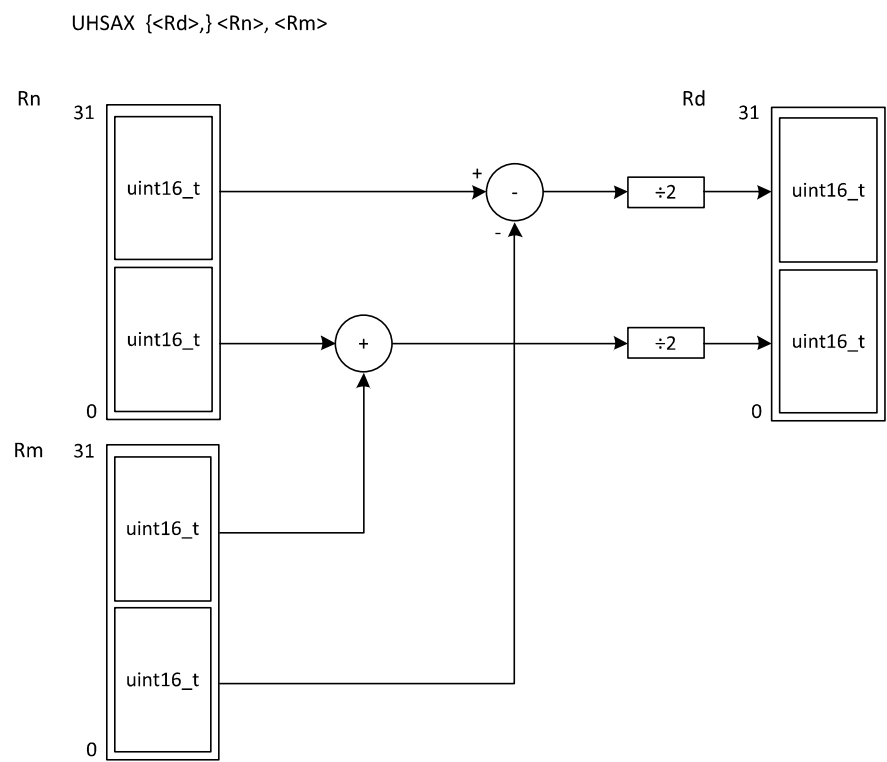


FIGURE B.80

UHSAX

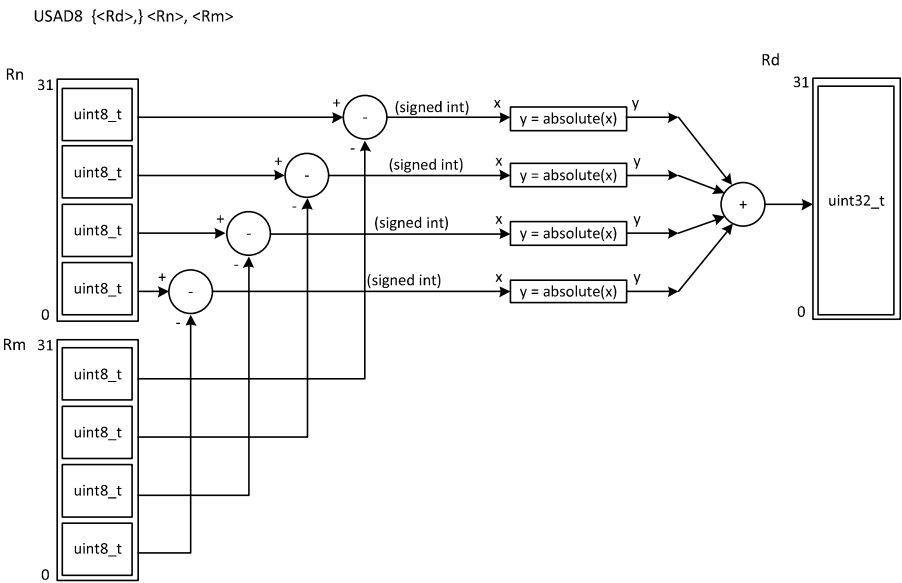


FIGURE B.81

USAD8

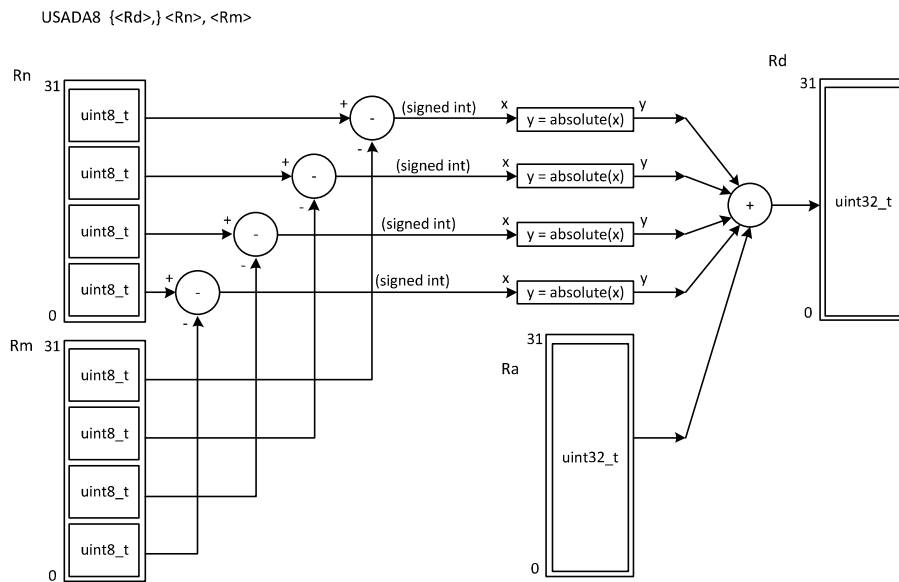


FIGURE B.82

USADA8

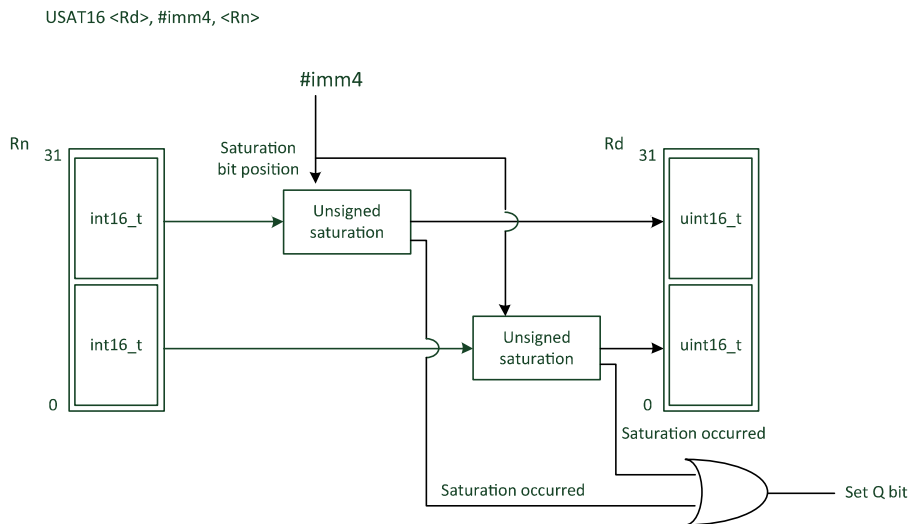


FIGURE B.83

USAT16

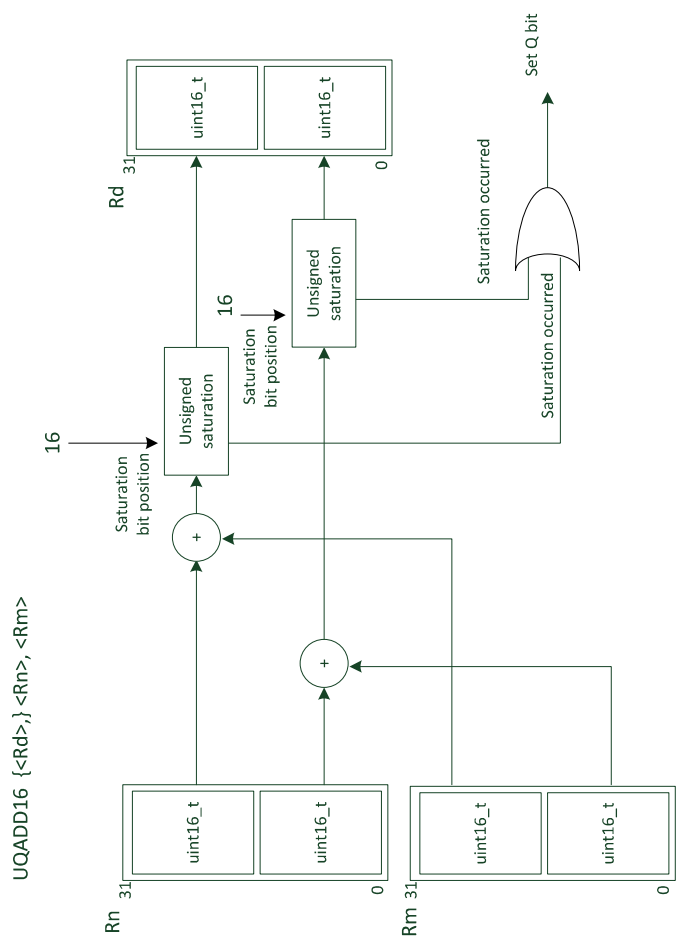


FIGURE B.84  
UQADD16

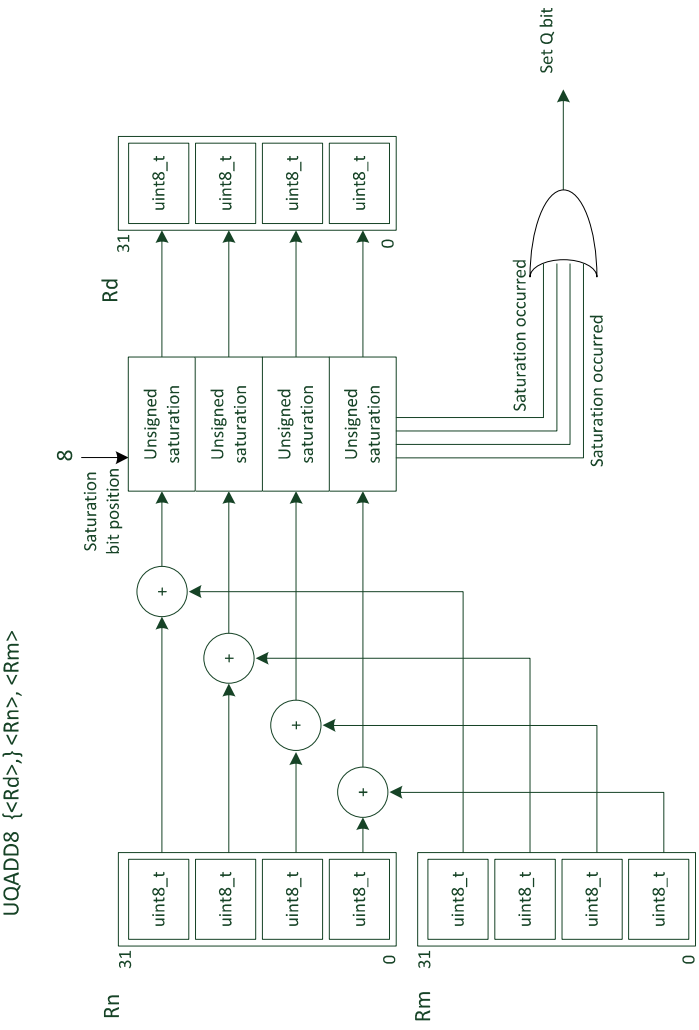


FIGURE B.85  
UQADD8



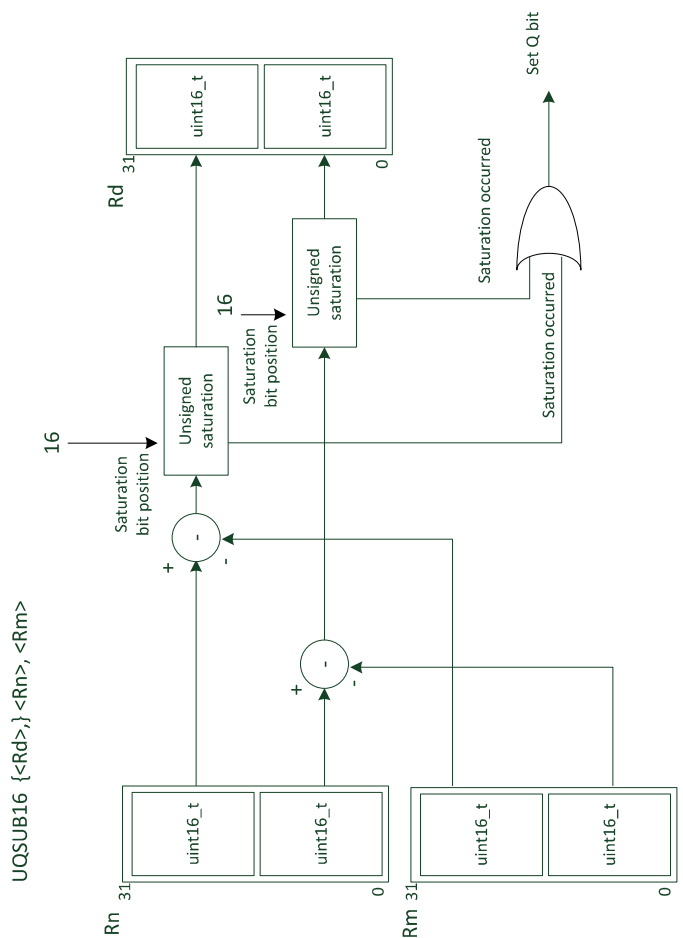


FIGURE B.86  
UQSUB16

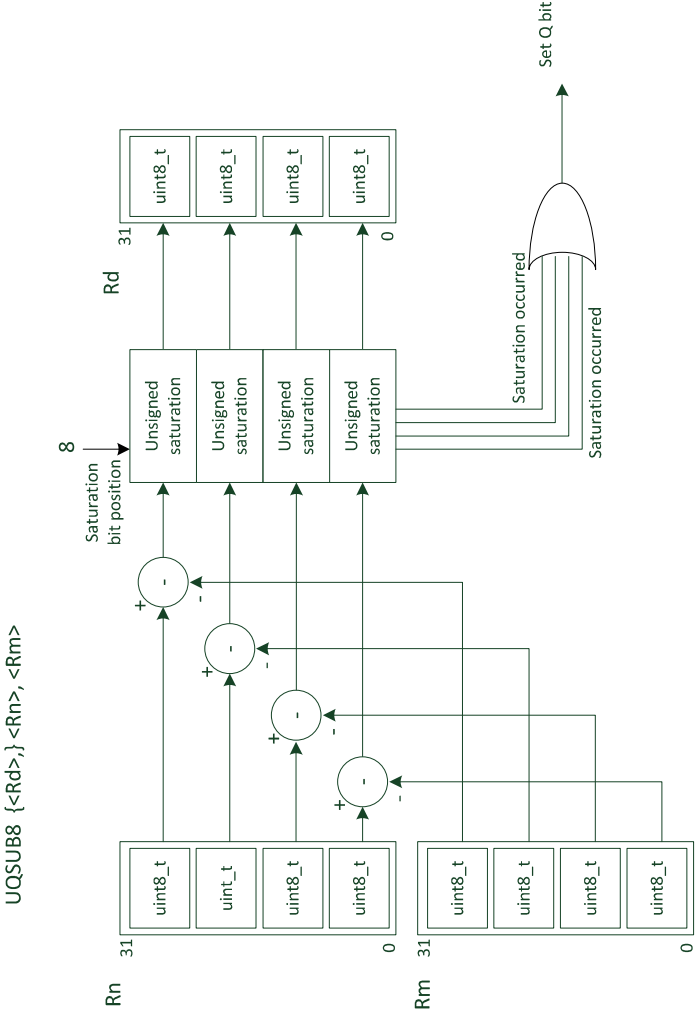


FIGURE B.87  
UQSUB8

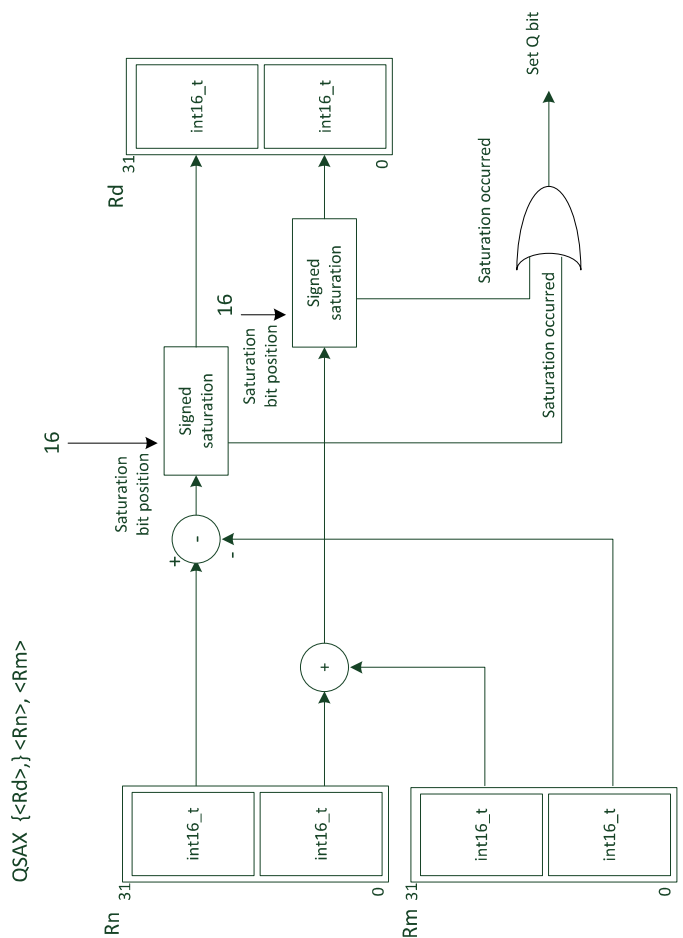


FIGURE B.88  
UQASX

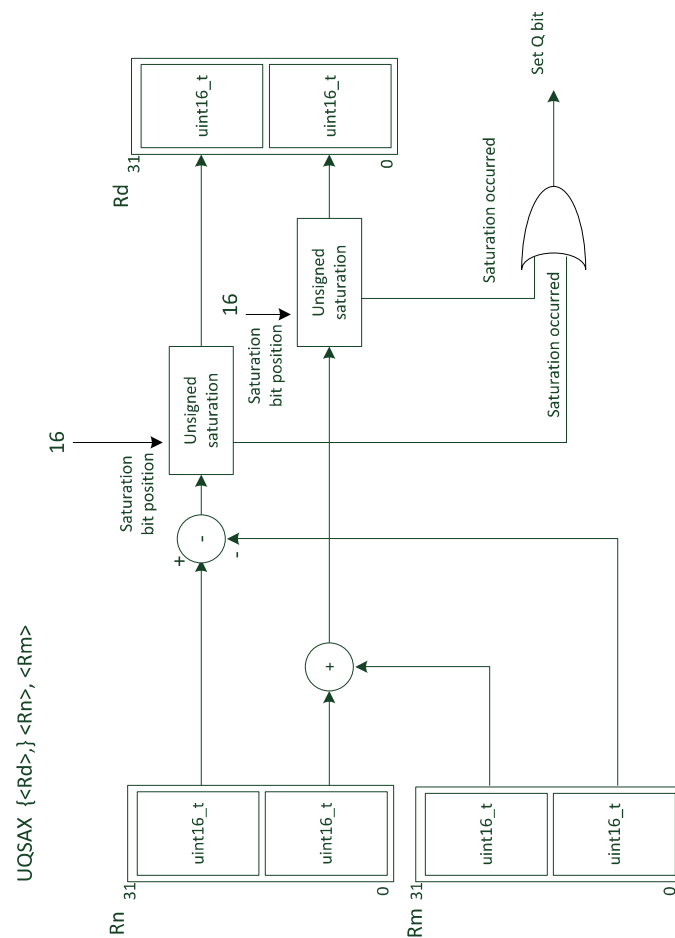
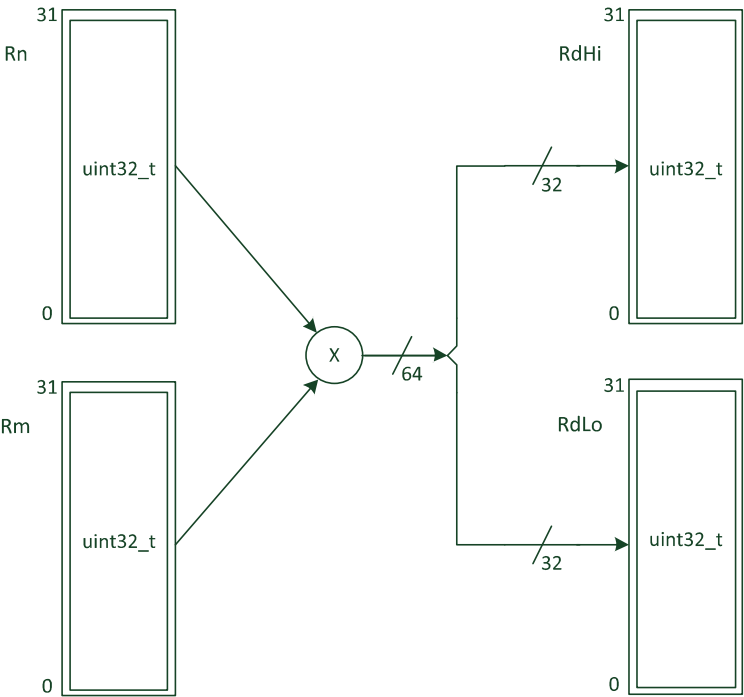


FIGURE B.89

UQSAX

UMULL <RdLo>, <RdHi>, <Rn>, <Rm>  
(available in the Cortex-M3)



**FIGURE B.90**  
UMULL

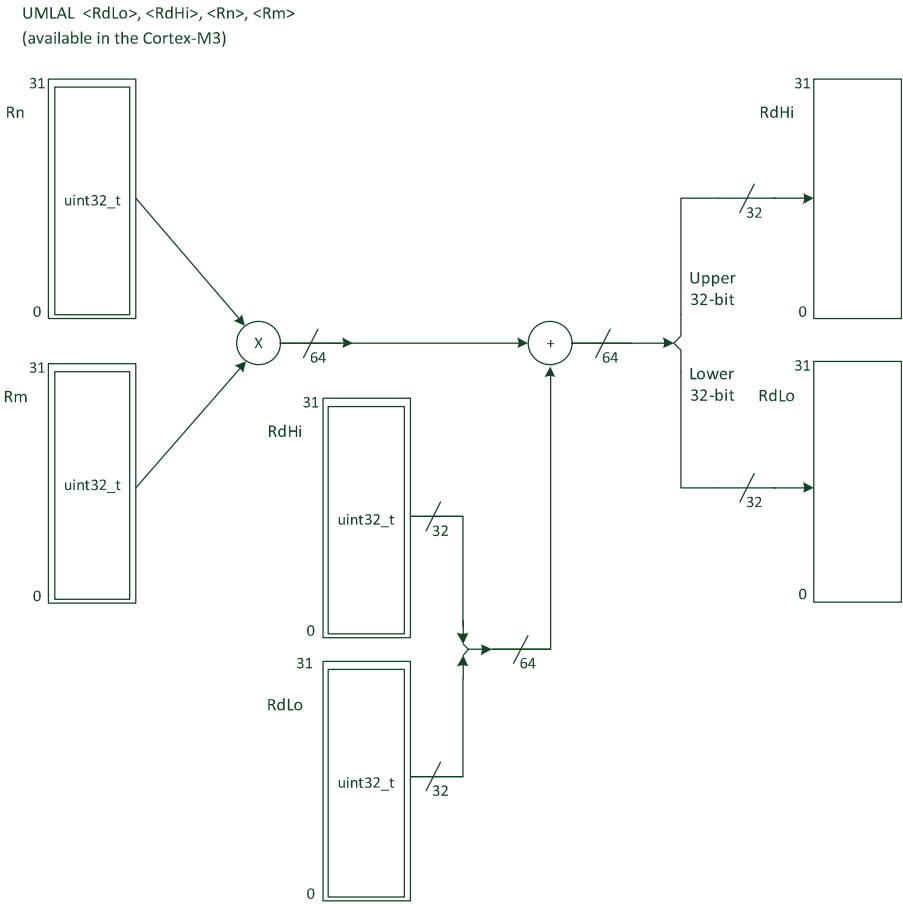


FIGURE B.91

UMLAL

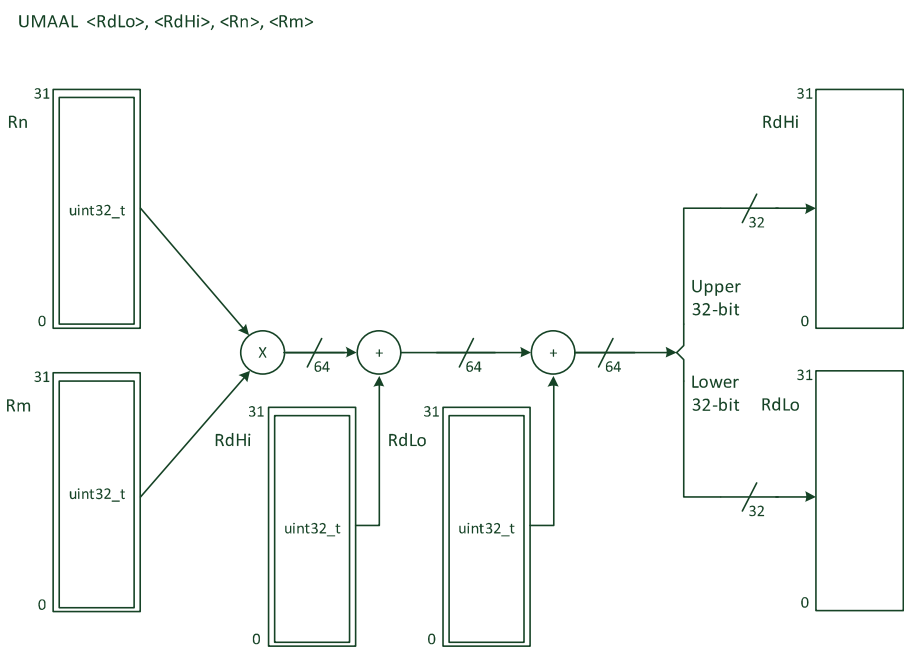


FIGURE B.92  
UMAAL

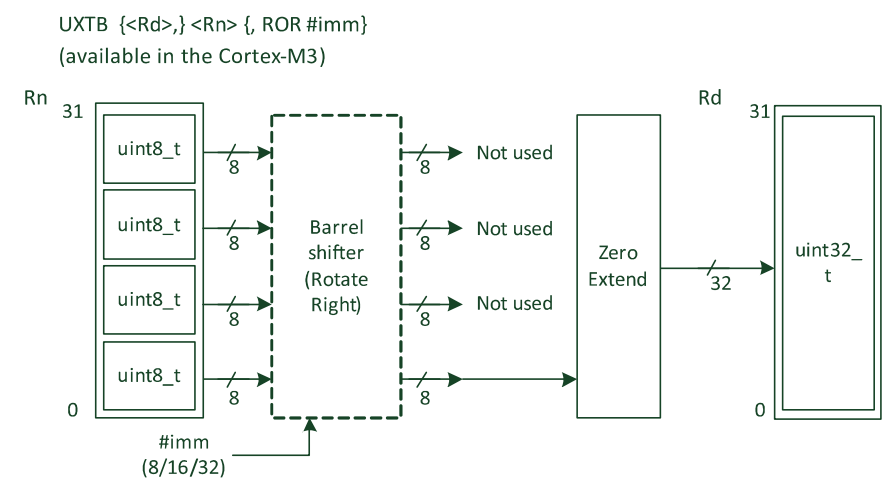


FIGURE B.93  
UXTB

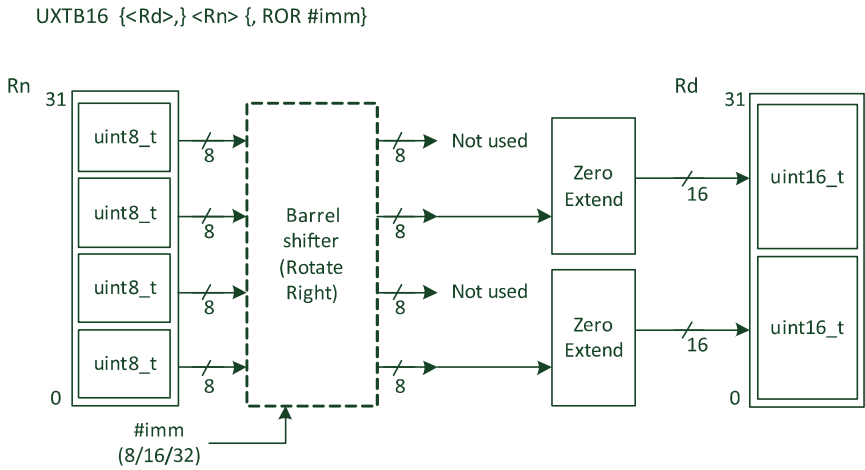


FIGURE B.94

UXTB16

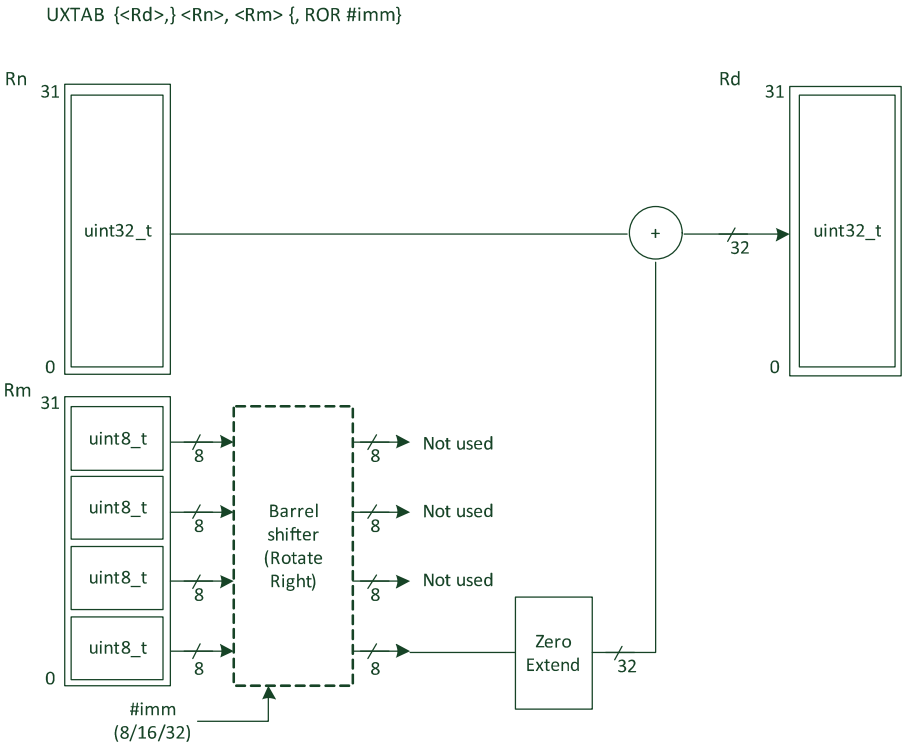


FIGURE B.95

UXTAB



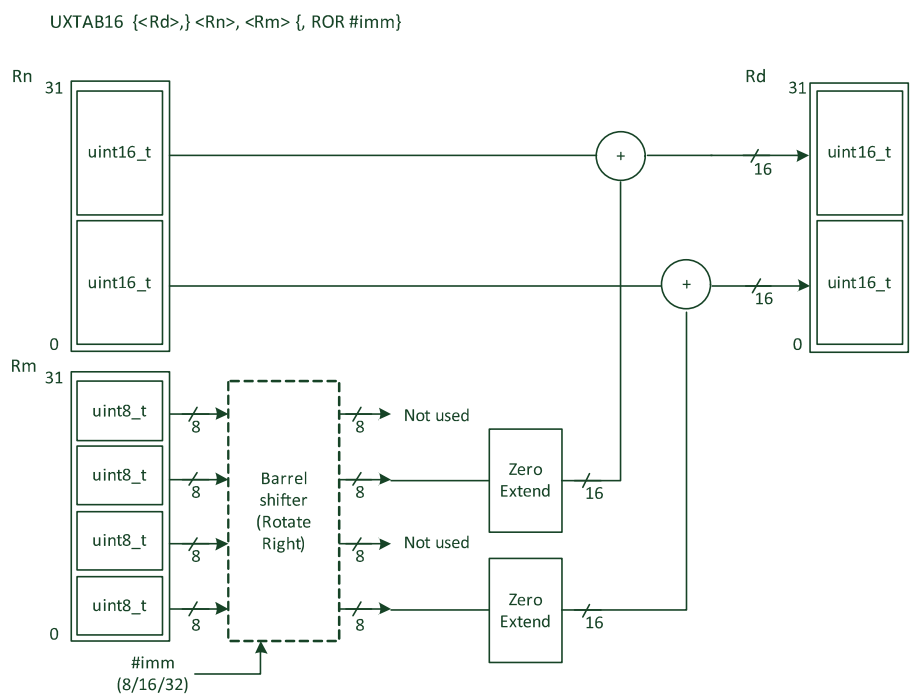


FIGURE B.96

UXTAB16

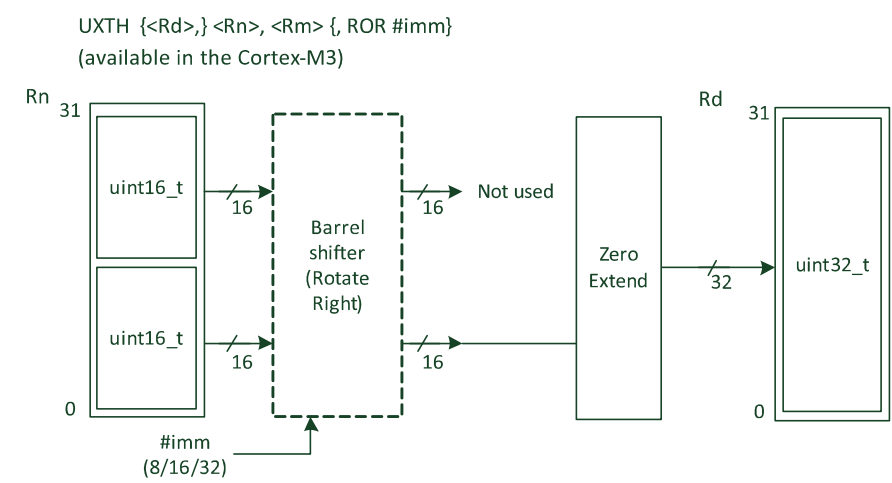
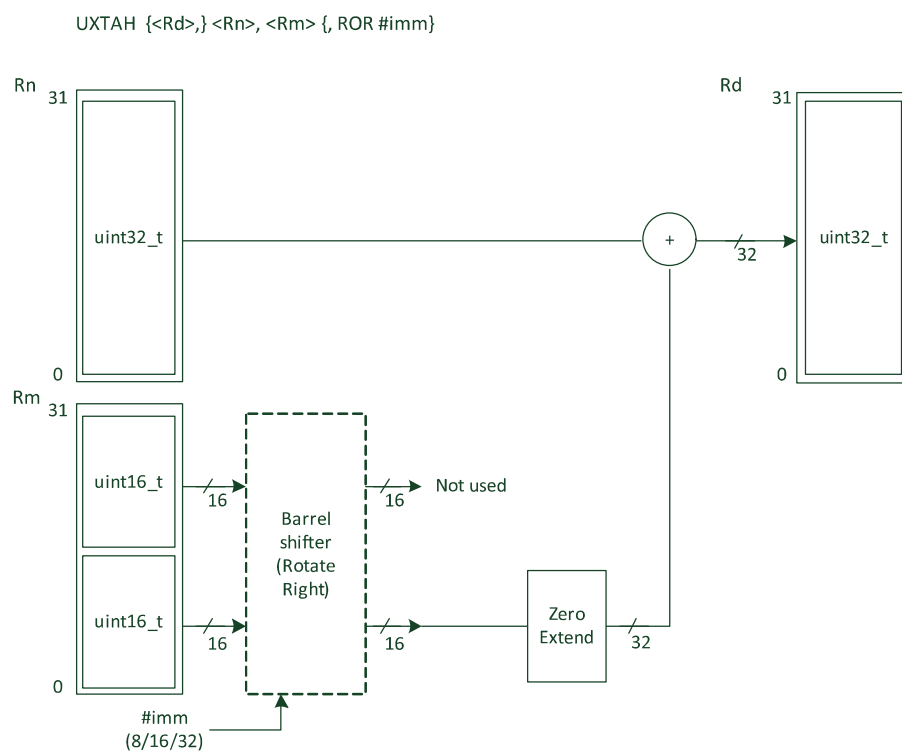


FIGURE B.97

UXTH



**FIGURE B.98**

UXTAH

## Addition of 16-bit Thumb<sup>®</sup> Instructions in Recent Architecture Versions

Most of the 16-bit Thumb<sup>®</sup> instructions are available in architecture v4T (ARM7TDMI<sup>™</sup>). However, a number of them are added in architecture v5, v6, and v7. [Table C.1](#) lists these instructions.

**Table C.1** Change of 16-bit Instruction Support in Various Recent ARM<sup>®</sup> Architecture Versions

| Instruction         | v4T | v5 | v6 | v6T2             | Cortex-M3/M4 (v7-M)      |
|---------------------|-----|----|----|------------------|--------------------------|
| BKPT                | N   | Y  | Y  | Y                | Y                        |
| BLX                 | N   | Y  | Y  | Y                | BLX ,reg. only           |
| CBZ, CBNZ           | N   | N  | N  | Y                | Y                        |
| CPS                 | N   | N  | Y  | Y                | CPSIE <i/f>, CPSID <i/f> |
| CPY                 | N   | N  | Y  | Y                | Y                        |
| NOP                 | N   | N  | N  | Y                | Y                        |
| IT                  | N   | N  | N  | Y                | Y                        |
| REV (various forms) | N   | N  | Y  | Y                | REV, REV16, REVSH        |
| SEV                 | N   | N  | N  | N <sup>(1)</sup> | Y                        |
| SETEND              | N   | N  | Y  | Y                | N                        |
| SWI                 | Y   | Y  | Y  | Y                | Changed to SVC           |
| SXTB, SXTB          | N   | N  | Y  | Y                | Y                        |
| UXTB, UXTB          | N   | N  | Y  | Y                | Y                        |
| WFE, WFI            | N   | N  | N  | N <sup>(1)</sup> | Y                        |

*Note 1: SEV, WFE and WFI executes as NOP in v6T2 (First implementation of Thumb 2 on ARM1156T2(F)-S<sup>™</sup>)*

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